LABORATORY WORK BOOK

Digital Logic Design

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CONTENTS

Introduction:

Binary logic consists of binary variables and logical operations. The variables are designated by letters of the alphabet such as *A, B,* C, *x, y,* z, etc., with each variable having two and only two distinct possible values: 1 and O. There are three basic logical operations: AND, OR, and NOT.

1. AND:. This operation is represented by a dot or by the absence of an operator. For example, *x. Y* = z or *xy* = z is read *"x* AND *y* is equal to *z."* The logical operation AND Js interpreted to, mean that z = 1 if and only if *x* = 1 *and Y* = 1; otherwise z = 0. (Remember that *x, y,* and z are binary variables and can be equal either to I or 0, and nothing else.)

2. OR: This operation is represented by a plus sign. For example, *x* + *y* = z is read *"x* OR *y*" is equal to *z,"* meaning that z = 1 if *x* = 1 *or* if *y* = 1 *or* if both *x* = 1 and *y* = 1. If both *x* and *y* = 0, then z = O.

3. NOT: This operation is represented by a prime (sometimes by a bar). For example, *x'* = z (or x = *i)* is read "not *x* is equal to 1.," meaning that z is what *x* is not. In other words, if *x* = 1, then z = 0; but if *x* = 0, then z = 1.

Binary logic resembles binary arithmetic, and the operations AND and OR have some similarities to multiplication and addition, respectively. In fact, the symbols used for AND and OR are the same as those used for multiplication and addition. However, binary logic should not be confused with binary arithmetic. One should realize that an arithmetic variable designates a number that may consist of many digits. A logic variable is always either a 1 or a O. For example, in binary arithmetic, we have 1 + 1 = 10 (read: "one plus one is equal to 2"), whereas in binary logic, we have 1 + I = I (read: “one OR one is equal to one”).

For each combination of the values of *x* and *y,* there a value of z specified by the definition of the logical operation. These definition may be listed in a compact form using *truth tables.* A truth table is a table of all possible combinations of the variables showing relation between the values that the variables may take and the result of the operation.

Experiment No 1

a.To check the operation of OR gate according to the OR's truth table, using the IC 74LS32.

Theory:

The electronic symbol for a two- input OR gate is shown in fig.1. The two inputs have been marked as A and B and the output as C. The OR gate has an output of 1when either A or B or both are 1.

In other words , It is any or all gate because an output occurs when any or all the inputs are present. Obviously, the output would be 0 if and only if both its inputs are 0. The OR gate represents the Boolean equation

A+B=C

The above logic operation of the OR gate can be summarized with the help of the truth table A truth table may be defined as a table which gives the output state for all possible input combinations. The truth table is also shown below.

Equipment Component:

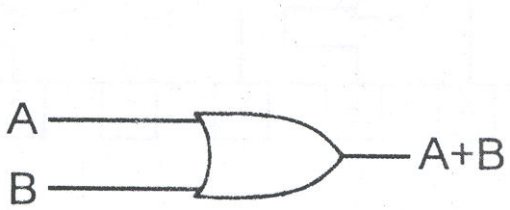
1. 74LS32 X 1

Tools:

2. EES – 2001 Trainer
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Symbolic Diagram:

Fig.1

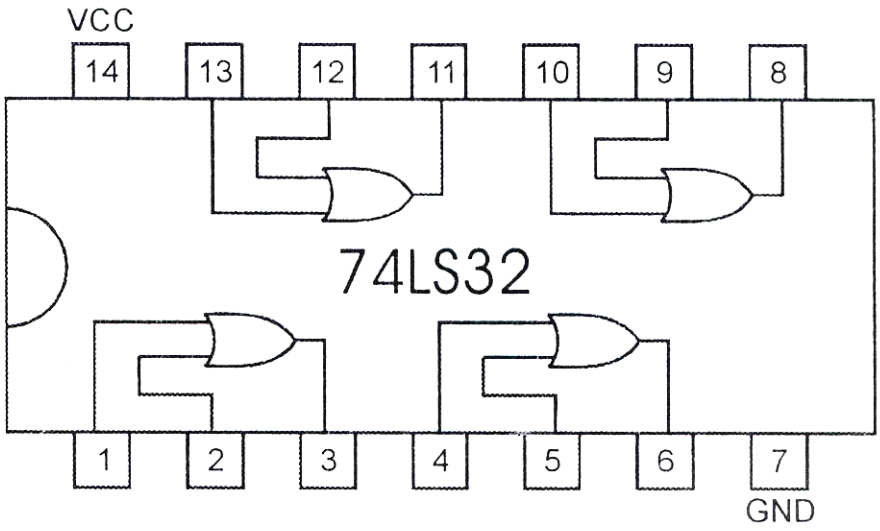


Truth Table:

Input		Out Put
A	**B**	**C=A+B**
0	0	0
0	1	1
1	0	1
1	1	1

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS32 on the trainers braced board.
4. Wire the circuit according to the diagram by consulting OR gate IC's data sheet.
5. Use and of the two logic switches S2 to SI for inputs to OR gate.
6. For output indication use any of the LED's form L_O – L_{I5}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combinations of inputs and verify the output according to the truth table of OR gate.



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

b.To check the operation of NOT gate according to the NOT's truth table, using the IC 74LS04.

Theory:

It is so called because its output is NOT same as its inputs. It is also called an inverter because it inverts the input signal. It has one input And one output. All it does to invert (or complement) the inputs seen from its truth table.

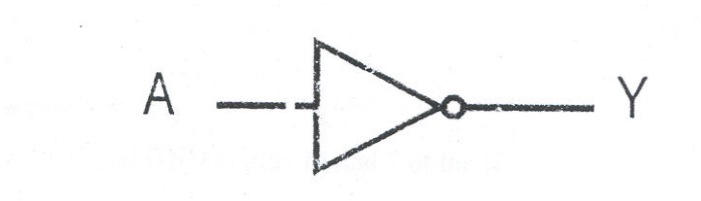
Equipment Component:

1. 74LS04 x 1

Tools:

1. EES – 2001 Trainer
2. Cutter
3. Single Core Wire
4. Tweezers
5. Pair of Pliers

Symbolic Diagram:

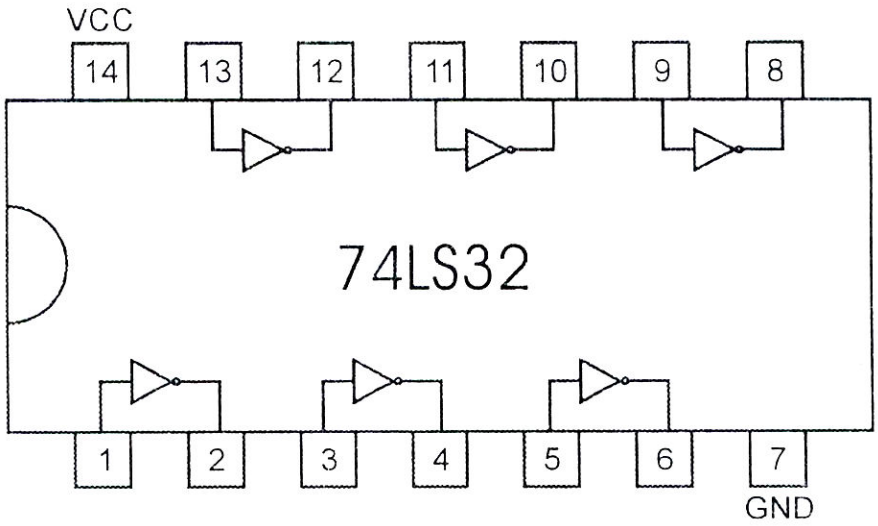


Truth Table:

In Put	Out Put
A	B
0	1
1	0

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS04 on the trainers braced board.
4. Wire the circuit according to the diagram by consulting NOT gate IC's data sheet.
5. Use and of the two logic switches S2 to SI for inputs to NOT gate.
6. For output indication use any of the LED's form L_O – L_{I5}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combinations of inputs and verify the output according to the truth table of NOT gate.



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

c.To check the operation of AND gate according to the AND's truth table, using the IC 74LS08.

Theory:

The logic symbol for 2-input AND gate is shown in Fig. 2 .A and B are two inputs .C is an output. They have value either 0or 1. The AND gate gives an output only when all its inputs are present. The AND gate has a 1 output only when both A and B are 1. Hence, this gate is an **all –or –nothing** gate whose outputs occur when all its outputs are present.

The AND gate represents the Boolean equation

A.B=C

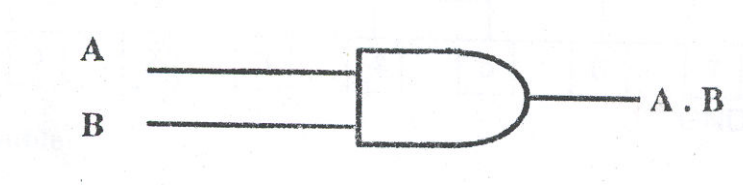
Equipment Component:

1. 74LS08 x 1

Tools:

1. EES – 2001 Trainer
2. Cutter
3. Single Core Wire
4. Tweezers
5. Pair of Pliers

Symbolic Diagram:



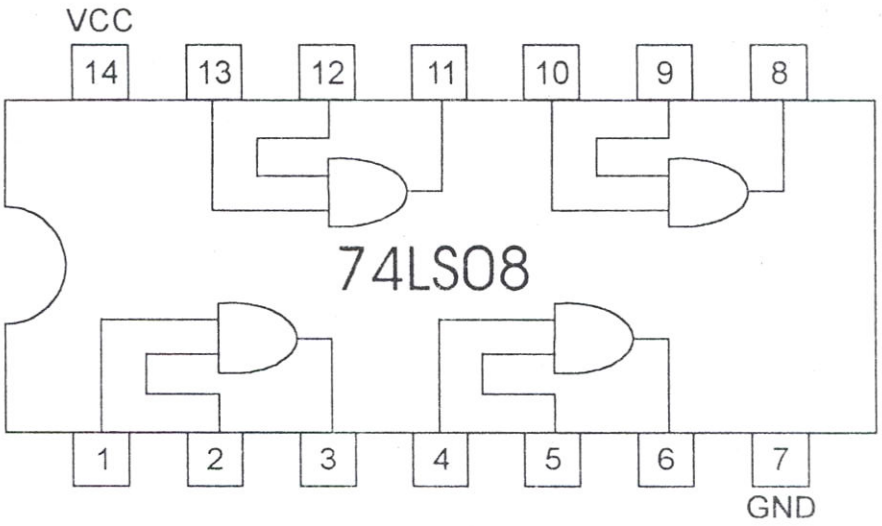
Truth table:

Input		Out Put
A	**B**	**C=A.B**
0	0	0
0	1	0
1	0	0
1	1	1

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.

2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS08 on the trainers braced board.
4. Wire the circuit according to the diagram by consulting AND gate IC's data sheet.
5. Use and of the two logic switches S2 to SI for inputs to AND gate.
6. For output indication use any of the LED's form L_O – L_{I5}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combinations of inputs and verify the output according to the truth table of AND gate.



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

d.To check the operation of NAND gate according to the NAND's truth table, using the IC 74LS00.

Theory:

It is in fact a NOT-AND gate .It can be obtained by connecting a NOT gate in the output of an AND gate as shown in fig. Its output is given by the Boolean equation.

C=(A.B)'

This gate gives an output if either A or B or both are 0.

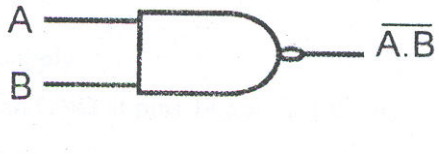
Equipment Component:

1. 74LS00 x 1

Tools:

1. EES – 2001 Trainer
2. Cutter
3. Single Core Wire
4. Tweezers
5. Pair of Pliers

Symbolic Diagram:



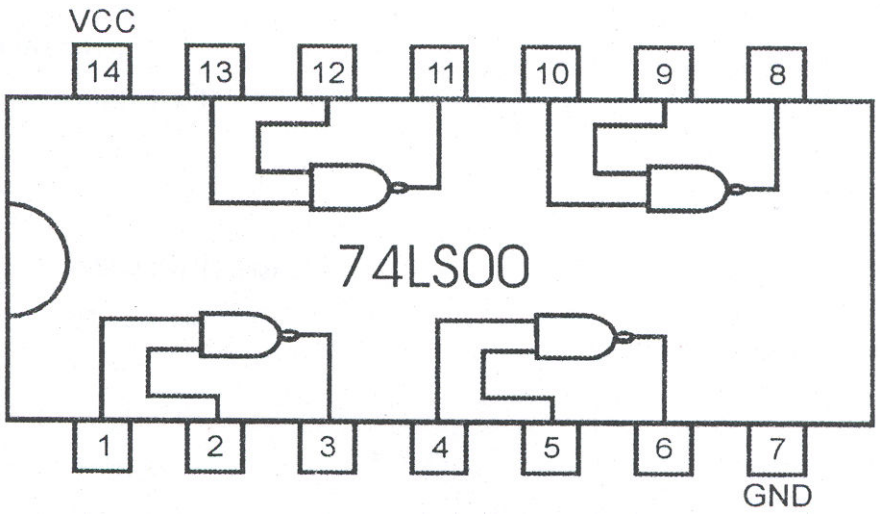
Truth table:

Input		Out Put
A	**B**	**(A.B)'**
0	0	0
0	1	0
1	0	0
1	1	1

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS00 on the trainers braced board.
4. Wire the circuit according to the diagram by consulting NAND gate IC's data sheet.
5. Use and of the two logic switches S2 to SI for inputs to NAND gate.

6. For output indication use any of the LED's form L_O – L_{I5}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combinations of inputs and verify the output according to the truth table of NAND gate.



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

e.To check the operation of NOR gate according to the NOR's truth table, using the IC 74LS02.

Theory:

It is a NOT-OR gate. It can be obtained by connecting a NOT gate in the output of an OR gate as shown in fig. Its output is given by the Boolean equation.

C= (A+B)′

It gives an output when its both inputs are 0.

Equipment:

Component

1. 74LS02 x 1

Tools

1. AM-2000 Trainer.
2. Cutter.
3. Single Core Wirez
4. Tweezer.
5. Pair of Pliers.

Symbolic Diagram:

Truth Table:

Input		Out Put
A	**B**	**(A+B)′**
0	0	1
0	1	0
1	0	0
1	1	0

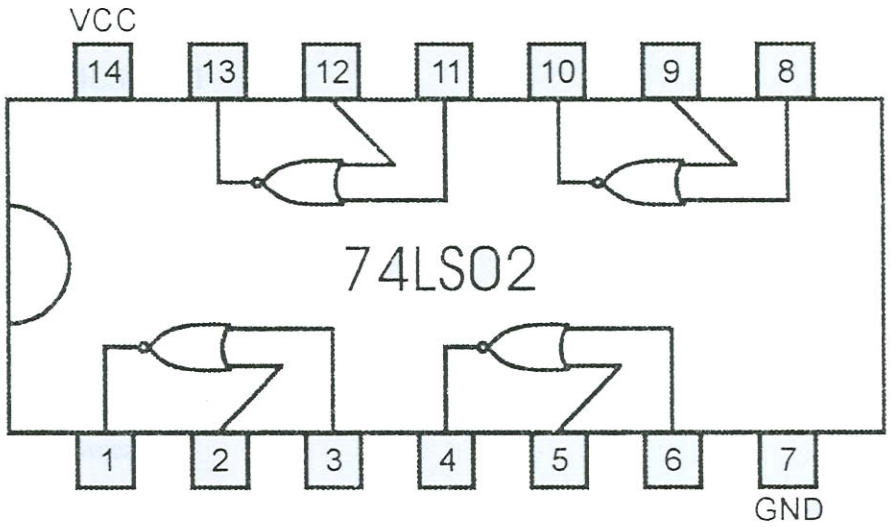
Procedure:

1. Connect the AM-2000 trainer to the 220 V AC power supply.

2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It

should be +5V exactly.

3. Install the IC 74LS02 on the trainer's breadboard.
4. Wire the circuit according to the diagram in fig. 6.1 by consulting NOR gate Ie's data sheet in fig.
5. Use any of the two logic switches from S2 to S9 for inputs to NOR gate.
6. For output indication use any of the LED's from (L_O - L_{I5}).
7. Supply the VCC= +5V and GND to the pins 14 and 7 of the Ie.
8. Test all the possible combinations of inputs and verify the output according to the truth table of NOR gate.



In Case of Trouble

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the Ie.
3. Check all the wire connections
4. Check the circuit wiring and remove the breaks.
5. Check the IC using. truth table.

f.To check the operation of XOR gate according to the XOR's truth table using IC 74LS86.

THEORY:

It is the gate which gives an output 1when its inputs are not same (or exclusive) and an output 0 when its inputs are same. It's symbol is shown in fig.

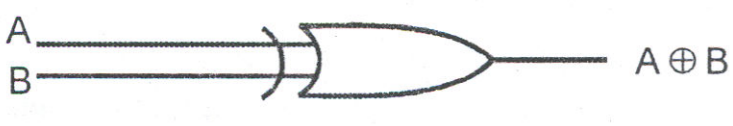
Equipment Component:

1. 74LS86 X 1

Tools:

1. EES – 2001 Trainer
2. Cutter
3. Single Core Wire
4. Tweezers
5. Pair of Pliers

Symbolic Diagram:

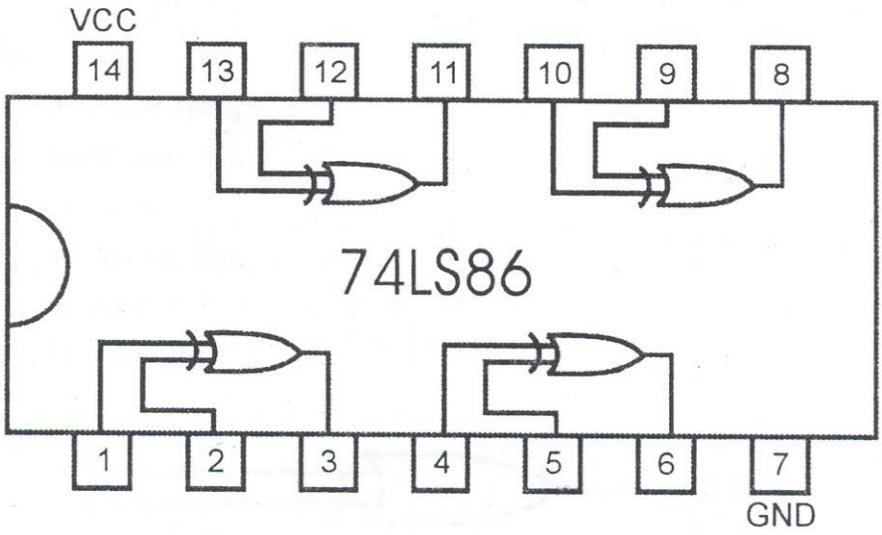


Truth table:

In Put		Out Put
A	**B**	**A +B**
0	0	0
0	1	1
1	0	1
1	1	0

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage.
3. Install the IC's 74LS86 on the trainers braced board.
4. Wire the circuit.
5. Use logic switches S2, SI for inputs.
6. For output indication use any of the LED from L_O – L_{15}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the IC.
8. Test all the possible combinations of inputs.



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring.
5. Check the IC using the truth table.

Experiment No 2

To check the operation of XOR gate, using IC74LS00.

Theory:

MULTILEVEL NAND CIRCUITS:

Combinational circuits are more frequently constructed with NAND or NOR gates rather than AND and OR gates. NAND and NOR gates are more common from the hardware point of view because they are readily available in integrated-circuit form. Because of the prominence of NAND and NOR gates in the design of combinational circuits, it is important to be able to recognize the relationships that exist between circuits constructed with AND-OR gates and their equivalent NAND or NOR diagrams.

The NAND gate is said to be a universal gate because any digital system can be implement with it. Combinational circuits and sequential circuits as well can be constructed with this gate because the flip-flop circuit (the memory element most frequently used in sequential circuits) can be constructed from two NAND gates. With the help of 4 NAND gate we can construct XOR gate as show in fig(A).

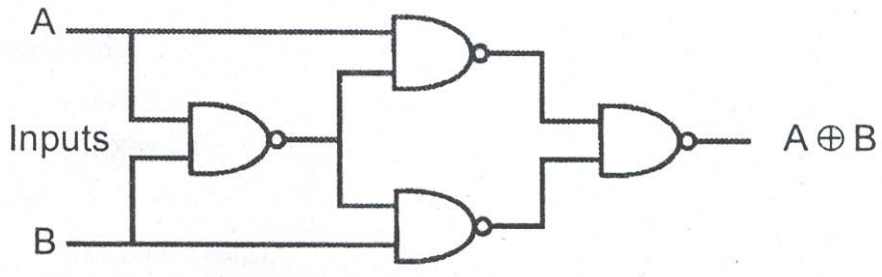
Equipment Component:

1. 74LS00 X 1

Tools:

1. EES – 2001 Trainer
2. Cutter
3. Single Core Wire
4. Tweezers
5. Pair of Pliers

Symbolic Diagram:



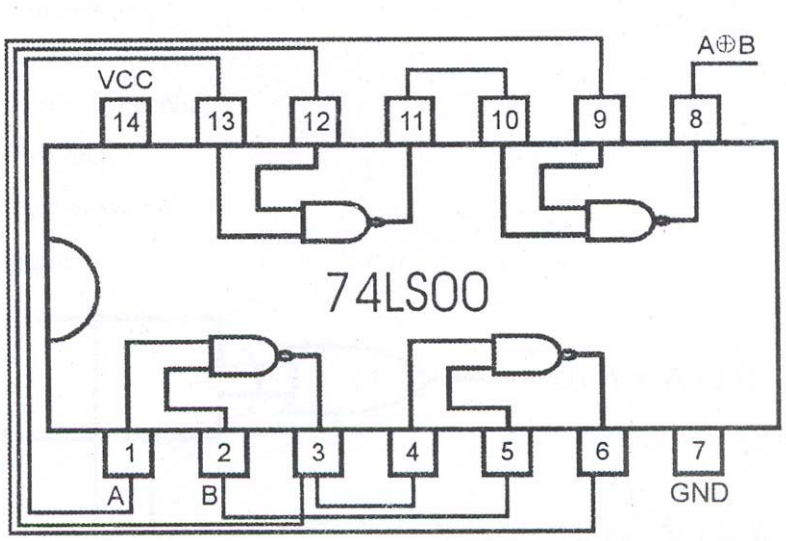
fig(A).

Truth table:

Input		Out Put
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS00 on the trainers braced board.
4. Wire the circuit.
5. Use and of the two logic switches S2 to SI for inputs.
6. For output indication use any of the LED's from $L_0 – L_{15}$.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the both IC.
8. Test all the possible combinations of inputs.



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using the truth table.

Experiment No 3

To check the operation of OR gate according to the NAND's truth table, using the IC 74LS00.

Theory:

The OR operation is achieved through NAND gate with additional inverters in each input. With the help of 3 NAND gates we can construct OR gate.

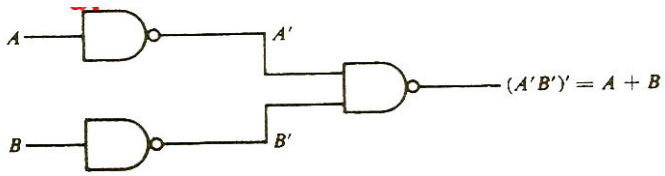
Equipment Component:

1. 74LS00 X 1

Tools:

1. EES – 2001 Trainer
2. Cutter
3. Single Core Wire
4. Tweezers
5. Pair of Pliers

Symbolic Diagram:

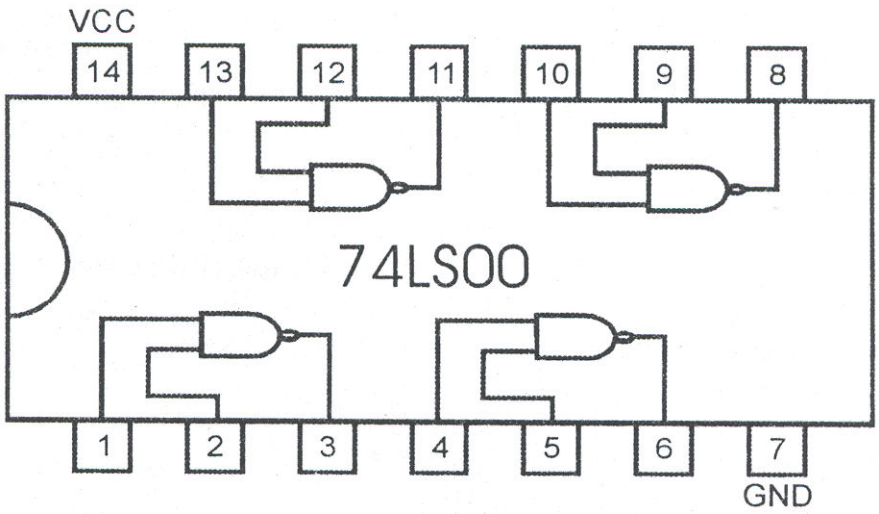


Truth Table:

Inputs		Out Put
A	B	(A+B)
0	0	0
0	1	1
1	0	1
1	1	1

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter.
3. Install the IC 74LS00 on the trainers braced board.
4. Wire the circuit.
5. Use and of the two logic switches S2 to SI for inputs.
6. For output indication use any of the LED's from L_0 – L_{15}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the both IC.
8. Test all the possible combinations of inputs.



In Case of Trouble:

2. Check the power supply.
3. Check the VCC and GND at pins 14 and 7 of the IC.
4. Check all the wire connections.
5. Check the circuit wiring and remove the breaks.
6. Check the IC using the truth table.

Experiment No 4

To check the operation of AND gate according to the NAND's truth table, using the IC 74LS00.

Equipment Component:

1. 74LS00 X 1

Tools:

1. EES – 2001 Trainer
2. Cutter
3. Single Core Wire
4. Tweezers
5. Pair of Pliers

Theory:

The AND operation requires two NAND gates. The first produces the inverted AND and the second acts as an inverter to produce the normal output.

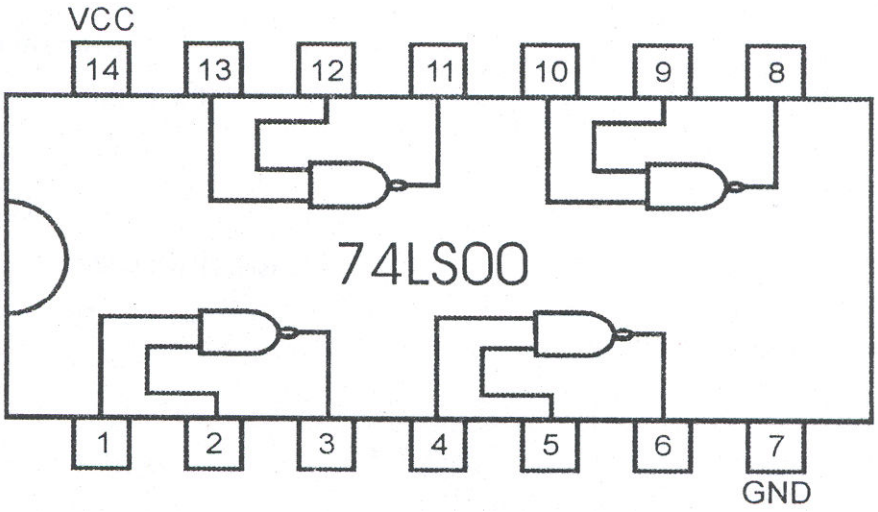
Symbolic Diagram:

Truth Table:

Input		Out Put
A	**B**	**((A.B)')'**
0	0	0
0	1	0
1	0	0
1	1	1

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply.
3. Install the IC 74LS00 on the trainers braced board.
4. Wire the circuit.
5. Use and of the two logic switches S2 to SI for inputs.
6. For output indication use any of the LED's from L_0 – L_{15}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the both IC.
8. Test all the possible combinations of inputs.



In Case of Trouble:

9. Check the power supply.
10. Check the VCC and GND at pins 14 and 7 of the IC.
11. Check all the wire connections.
12. Check the circuit wiring and remove the breaks.
13. Check the IC using the truth table.

Experiment No 5

To check the operation of NOT gate according to the NAND's truth table, using the IC 74LS00.

Equipment Component:

1. 74LS00 X 1

Theory:

The NOT operation is obtained from a one-input NAND gate, actually another symbol or an inverter circuit. A single NAND also works as a NOT gate.

Tools:

1. EES – 2001 Trainer
2. Cutter
3. Single Core Wire
4. Tweezers
5. Pair of Pliers

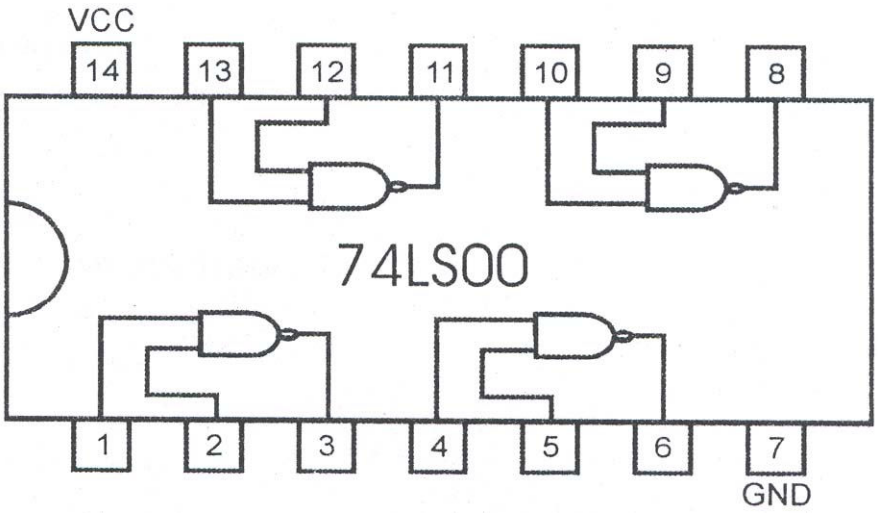
Symbolic Diagram:

Truth Table:

In Put	Out Put
A	(A)'
0	1
1	0

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply.
3. Install the IC 74LS00 on the trainers braced board.
4. Wire the circuit.
5. Use and of the two logic switches S2 to SI for inputs.
6. For output indication use any of the LED's from L_0 – L_{15}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the both IC.
8. Test all the possible combinations of inputs.



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using the truth table.

Combinational Logic circuits:

Introduction:

Logic circuits for digital systems may be combinational or sequential. A combinational circuit consists of logic gates. whose outputs at an time are determined directly from there the present combination of inputs Without regard_to previous Inputs. A combinational circuit performs a specific information-processing operation fully specified logically by a set of Boolean functions. Sequential circuits employ memory elements (binary cells) in addition to logic gates. Their outputs are a function of the_Inputs and the state of the memory elements. The state of memory elements, In turn, is a function of previous inputs. As a consequence, the outputs of a sequential circuit depend not only on present inputs, but also on past inputs, and circuit behavior must be specified by a time sequence of inputs and internal_state.
A combinational circuit consists of in variables. logic gates. and output variables. The logic gates accept signals from the inputs and generate signals to the outputs. This process transforms binary information from the given input data to the required output data. Obviously, both input and output data are represented by binary signals, i.e., they exist in two possible values, one representing logic-I. and the other logic-0.

Experiment No 6

To check the half adder operation using XOR and AND gates.

Theory:

Adders

Digital computers perform a variety of information-processing tasks. Among the basic functions encountered are the various arithmetic operation. The most basic arithmetic operation, no doubt, is the addition of two binary digits. This simple addition consists of four possible elementary operations, namely, 0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1,and 1 + 1 = 10. The first three operations produce a .sum whose length is one digit, I b but when both augends and addend bits are equal to 1, the binary sum consists of two digits. The higher significant bit of this result is called a *carry.* When the augends and addend numbers contain more significant digits, the carry obtained for the addition of two bits is added to the-next higher-order pair of significant bit.

Half Adder

A combinational circuit that performs the addition of two bits is called a *half-adder.* One that performs the addition three bits (two significant bits and a previous carry) is a f*ull-adder.* The two adder circuits are the first combinational circuits we shall design.
From the verbal explanation of a half-adder, we find that this circuit needs two binary inputs and two binary outputs. The input variables, designate the augends and addend bits; the output variables produce the sum and carry. It is necessary to specify two output variables because the result may consist of two binary digits. We arbitrarily assign symbols *x* and *y* to the two inputs and S (for sum) and C (for carry) to the outputs.

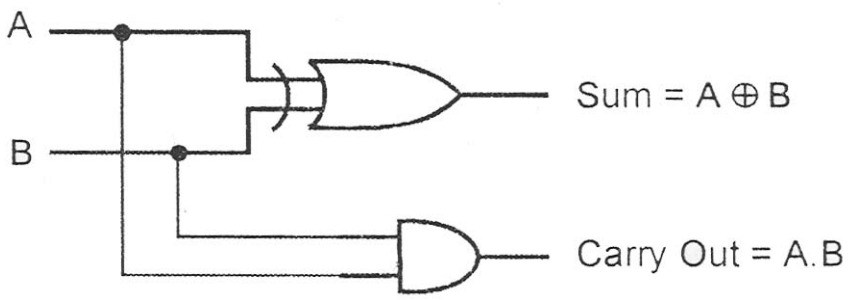
Equipment Component:

1. 74LS86 X 1
2. 74LS08 X 1

Tools:

1. EES – 2001 Trainer
2. Cutter
3. Single Core Wire
4. Tweezers
5. Pair of Pliers

Symbolic Diagram:

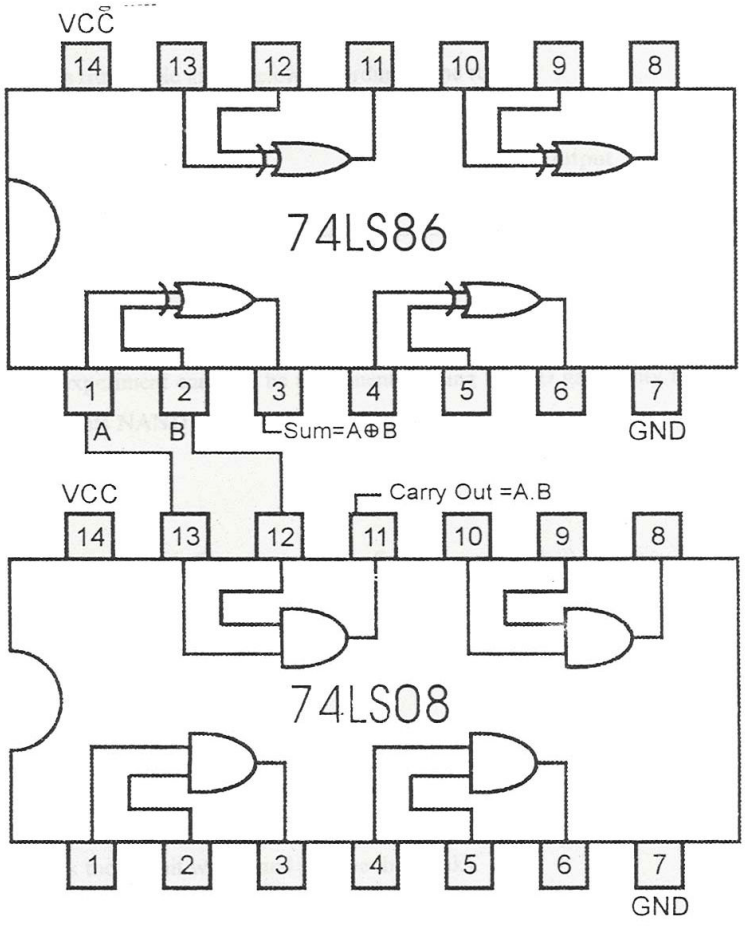


Truth Table:

In Put			Out Put
A	**B**	**Sum**	**A . B**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install the IC 74LS86 and IC 74LS08 on the trainers braced board.
4. Wire the circuit according to the diagram by consulting both IC's.
5. Use any of the two logic switches S2 to SI for inputs.
6. For output sum use LED L_O and for output carry, use LED L_1.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the both IC's.
8. Test all the possible combinations of inputs and verify the output according to the truth table of half adder.



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC's using their respective data sheets.

Experiment No 7

To design full adder circuit using XOR, AND & OR gates.

Theory:

Full Adder

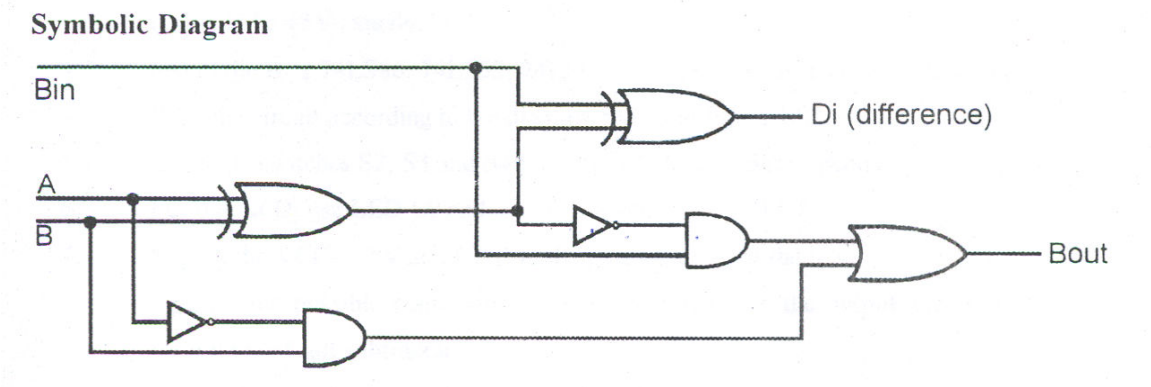
A full-adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by *x* and *y,* represent the two significant bits to be added. The third input, z, represents the carry from the previous lower significant position. Two outputs are necessary because the arithmetic sum of three binary digits ranges in value from 0 to 3, and binary 2 or 3 needs two digits. The two outputs are designated by the symbols *S* for sum and C for carry. The binary variable S gives the value of the least significant bit of the sum.

Equipment Component:

1. 74LS08 X 1
2. 74LS86 X 1
3. 74LS32 X 1

Tools:

1. EES – 2001 Trainer
2. Multimedia
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers



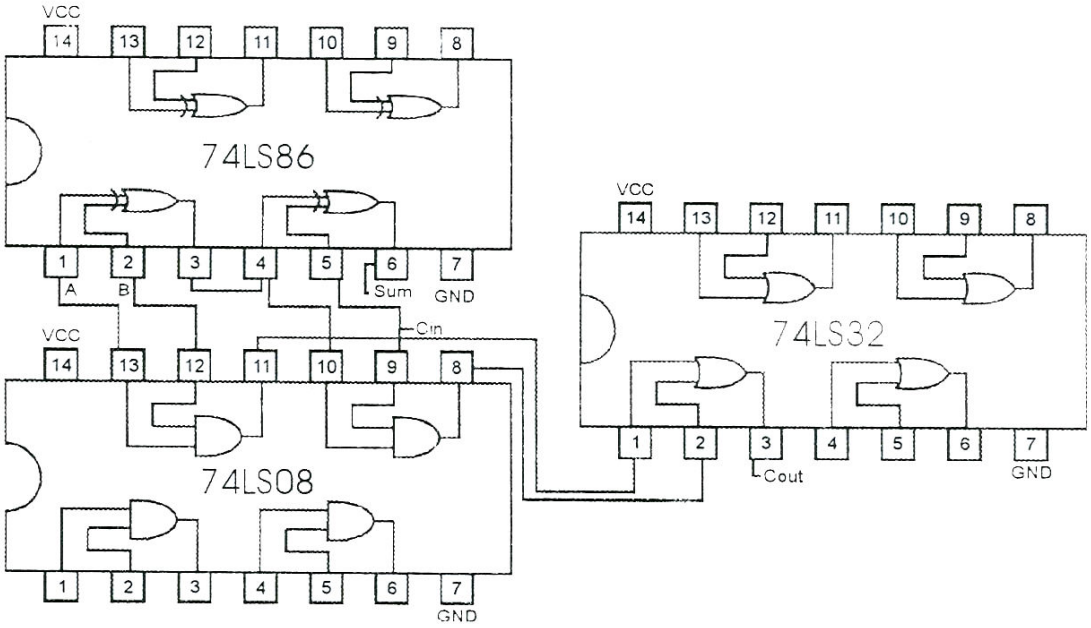
Truth Table:

In Puts			Out Puts	
A	**B**	**C**	**S**	**Cout**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**
0	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**1**

1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply using the multimeter.
3. Install the IC's 74LS08, 74LS86 and 74LS32 on the trainers braced board.
4. Wire the circuit according to the diagram by consulting IC.
5. Use logic switches S2, S3 and S4 for inputs A, B and C.
6. For output sum use LED L_0 and for output carry use LED L_1.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the both IC.
8. Test all the possible combinations of inputs verify the output according to the truth table.



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC.
3. Check all the wire connections.
4. Check the circuit wiring.
5. Check the IC using the data sheets.

Experiment No 8

To design half sub tractor circuit using XOR, AND & NOT gates.

Theory:

Sub tractors

The subtraction of two binary numbers may be accomplished by taking the complement of the subtrahend adding. By this method, the subtraction operation becomes an addition operation requiring full-adders for its machine implementation. It is possible to implement subtraction with logic circuits in a direct manner. By this method, each subtrahend bit number is subtracted from its corresponding significant minuend bit to form a difference bit. If the minuend-bit is smaller than the subtrahend bit, a 1 is borrowed from the next significant position. The fact that a 1 has been borrowed must be conveyed to the next higher pair of bits by means of a binary signal coming out (output) of a given stage and going into (input) the next higher stage. Just as there are - half- and full-adders, there are half- and full-subtractions.

Half-Sub tractor

A half sub tractor is a combinational circuit that subtracts two bits and produces their difference. It also has an output to specify if a 1 has been borrowed. Designate the minuend bit by x and the subtrahend bit by *y.* To perform *x - y,* we have to check the relative magnitudes of *x* and *y.* If *x ~ y,* we have three possibilities: 0 - 0 = 0, 1 - 0 = 1, and 1 - 1 = O. The result is called the *difference bit.* If *x < y,* we have 0 - 1, and 'it is necessary to borrow a 1 from the next higher stage. The 1 borrowed from the next higher stage adds 2 to the minuend bit, just as in the decimal system a borrow adds, 10 to a minuend digit. With the minuend equal to 2, the difference becomes 2 - 1 = 1. The half-sub tractor needs two outputs. One output generates the difference and will be designated by the symbol *D.* The second output, designated *B* for borrow, generates the binary signal that informs the next stage that a 1 has been borrowed.

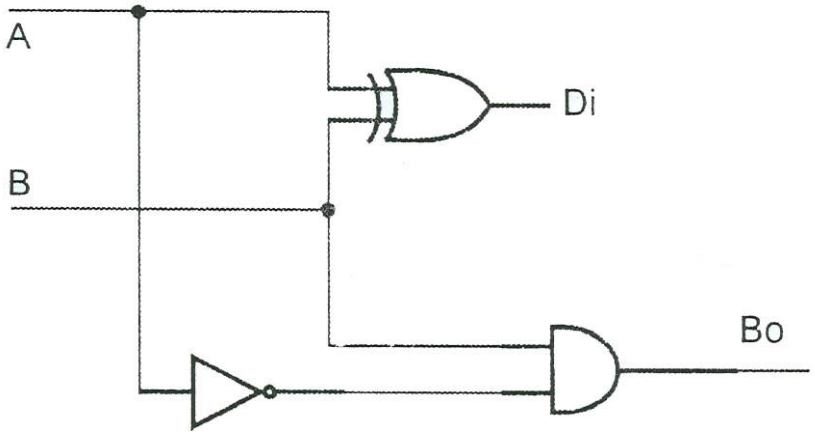
Equipment Component:

1. 74LS86 X 1
2. 74LS08 X 1
3. 74LS04 X 1

Tools:

1. EES – 2001 Trainer
2. Multimedia
3. Cutter
4. Single Core Wire
5. Tweezers
6. Pair of Pliers

Symbolic Diagram:



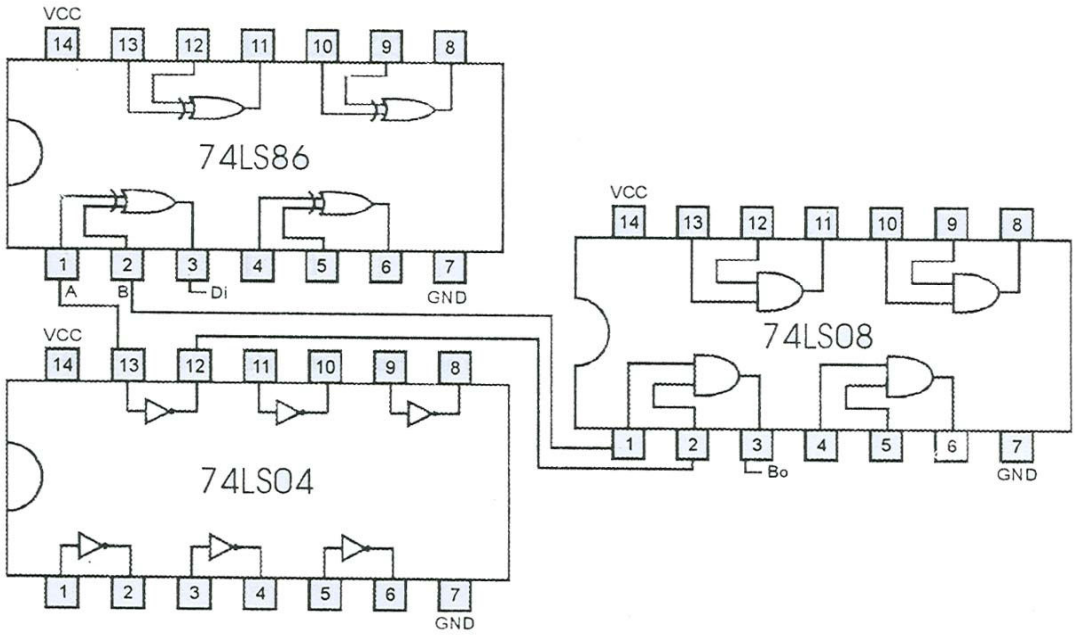
Truth Table:

In Put		Out Put	
A	**B**	**B_0**	**D_i**
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply.
3. Install the IC's 74LS08, 74LS86 and 74LS04 on the trainers braced board.
4. Wire the circuit.
5. Use logic switches S2 to SI for two inputs.
6. For output indication use any LED from L_O – L_{15}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the both IC's.
8. Test all the possible combinations of inputs verify the output.

Circuit Diagram



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC's.
3. Check all the wire connections.
4. Check the circuit wiring.
5. Check the IC's using the data sheets.

Experiment No 9

To check the full sub tractor circuit using XOR, AND , NOT and OR gates.

Theory:

Full Sub tractor

A full-sub tractor is a combinational circuit that performs a subtraction between two bits, taking into account that a 1 may have been borrowed by a lower significant stage. The circuit has three inputs and two outputs. The three inputs, *x, y,* and z, denote the minuend, subtrahend, and previous borrow, respectively. The two outputs, D and *B,* represent the difference and output borrows respectively.

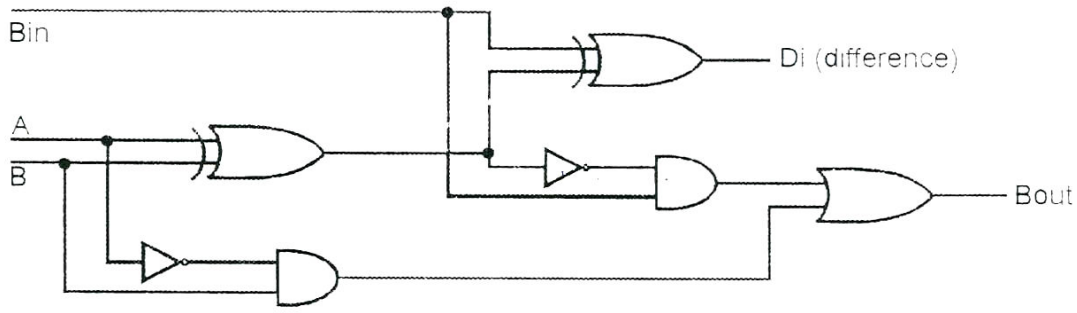
Tools:

1. EES – 2001 Trainer
2. Multimedia
3. Cutter
4. Single Core Wire
5. Tweezers

Equipment Component:

1. 74LS86 x 1
2. 74LS08 x 1
3. 74LS04 x 1
4. 74LS32 x 1

Symbolic Diagram



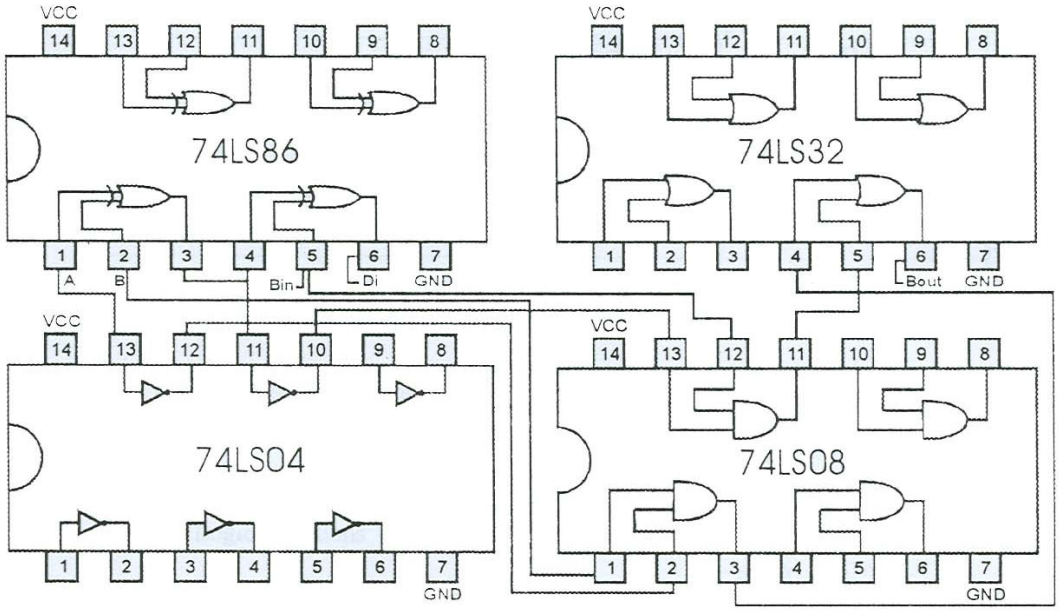
Truth Table:

In Put			Out Put	
A	**B**	**B_{in}**	**B_{out}**	**D_i**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Procedure:

1. Connect the EES – 2001 trainer to the 220V AC power supply.
2. Turn on the trainer and verify the voltage of the power supply.
3. Install the 4 IC's on the trainer's braced board.
4. Wire the circuit.
5. Use logic switches S2 to S3 and S4 for inputs.
6. For output indication use any LED from L_O – L_{15}.
7. Supply the VCC = +5V and GND to the pins 14 and 7 of the both IC's.
8. Test all the possible combinations of inputs.

Circuit Diagram



In Case of Trouble:

1. Check the power supply.
2. Check the VCC and GND at pins 14 and 7 of the IC's.
3. Check all the wire connections.
4. Check the circuit wiring.
5. Check the IC's using the data sheets.

Introduction

Combinational logic circuit

(1) In combinational logic circuit the output of the logic circuit depends only on the present input combinations
(2) No matter the inputs are change in any order, the outputs will remain the same for a particular input combination.
(3) AND , OR , NOT , NAND , & NOR gates are considered to be the combinational logic circuits

Sequential Logic circuit

(4) In sequential logic the output depend not only on the present input combinations but also on the past state of the output.
(5) The output depends on the sequence in which the inputs are changed.
(6) Sequential circuits involve some form of timing in their operation. The timing function permits one or several devices to be actuated at an appropriate time or an operational sequence. Sequential logic circuit consists of,
(1) Combinational circuit
(2) Memory Element.

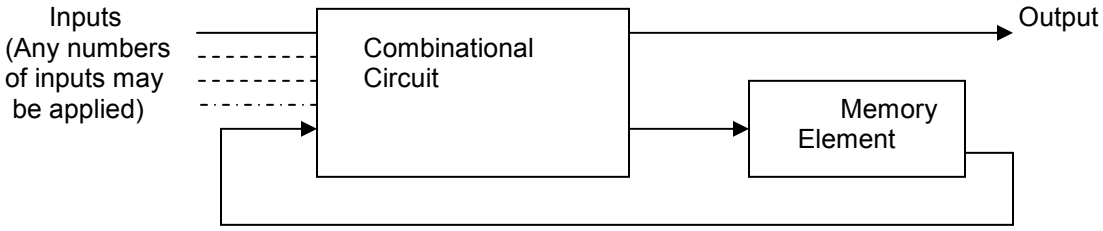
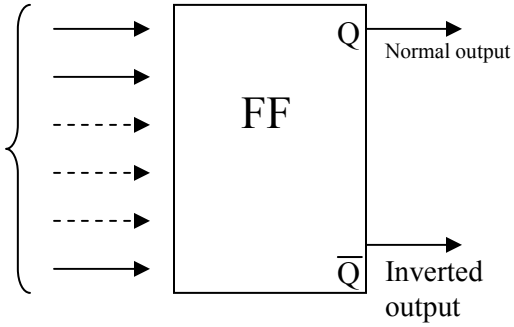


Fig 1

The memory elements used in sequential logic are called Flip – flop or Latch or Binary Sequential logic is used in Register & counters.

Symbol For A Flip – flop

A general type of symbol used for a flip-flop is shown in fig.2 it has two outputs & inputs labeled Q & $\overline{Q}$ which are the inverse of each other. The Q output is called the normal output and Q is the inverted output. If we say that the Flip – flop is in the High – state, we mean that Q = 1 & if we that a flip – flop is in low – state we mean that Q = 0 of course, the Q state will always be the inverse of Q.



The high state i.e. Q = 1 & $\overline{Q}$ = 0 of a Flip – flop is also known as SET state. The low state i.e. Q = 0 & $\overline{Q}$ = 1 is then called RESET state. The reset state is also called the clear state.
The basic Latch or Flip – flop is RS Flip – Flop.

Simple Definition of FF

1. A FF is a logic circuit that consists of two inverters. Output of one-inverter acts as input of the other and vice verses.
2. They can store one (1) bit of information.
3. Normally FFs has two outputs, which are complements of each other.
4. Different FFs differ from each other in the no. of inputs & the inverse in which the inputs are applied to them.

Experiment No 10

To check the operation of basic RS- flip flop using IC 74LS00.

Equipment:

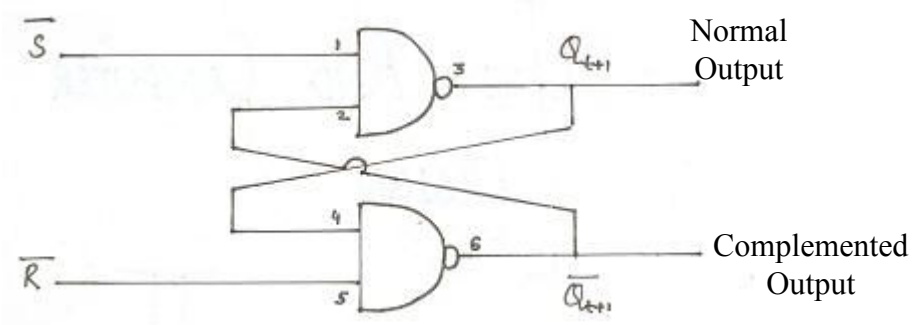
1. 74LS00 x 1
2. EES – 2001 trainer.
3. Cutter.
4. Tweezers
5. Single Core Wires.

Theory:

The basic latch or flip flop is called basic RS flip-flop.

1. A flip-flop is a logic circuit that consists of two invertors. Output of one-inverter acts as an input of the other.
2. They can store 1 bit input of information.
3. FFs have two outputs, which are complement of each other.

Symbolic Diagram:



Truth Table:

S′	R′	Q_{t+1}	Q_{t+1}′
0	1	0	1
0	0	0	1
1	0	1	0
0	0	1	0
1	1	1	0

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 11

To check the operation of clocked RS flip- flop using IC 74LS00.

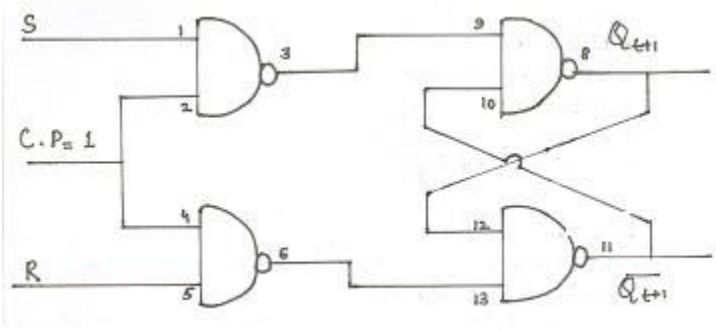
Equipment:

1. 74LS00 x1
2. EES – 2001 trainer.
3. Cutter.
4. Tweezers
5. Single Core Wires.

Theory

The operation of basic flip-flop can be modified by providing an additional control input that determines when the state of the circuit is to be changed .An RS-flip flop with a clock pulse input is shown. It consts of basic flip-flop circuit and two additional gates.

Symbolic Diagram:



Truth Table:

S	R	Q_{t+1}	Q_{t+1}'
0	1	0	1
0	0	0	1
1	0	1	0
0	0	1	0
1	1	1	1

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 12

To check the operation of D-Type flip-flop using NAND IC 74LS00.

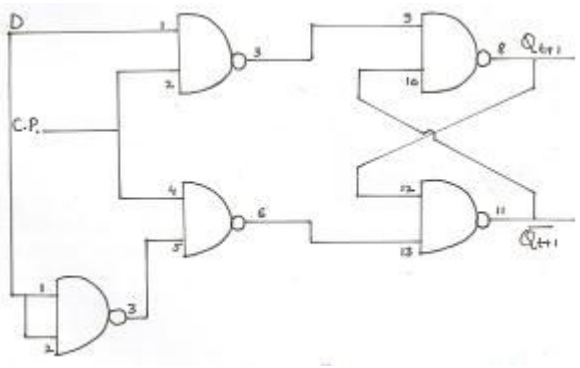
Theory:

The D-Type flip flop is a modification of the clocked RS flip-flop. D stands for data or delay. This flip-flop is used for data transfer.

Equipment:

1. 74LS00 x 1
2. EES – 2001 traner.
3. Cutter.
4. Tweezers
5. Single Core Wires.

Symbolic Diagram:



Truth Table:

D	Q_{t+1}	Q_{t+1}'
0	0	1
1	1	0

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 13

To check the operation of J – K flip-flop using IC 74LS00 and 74LS10

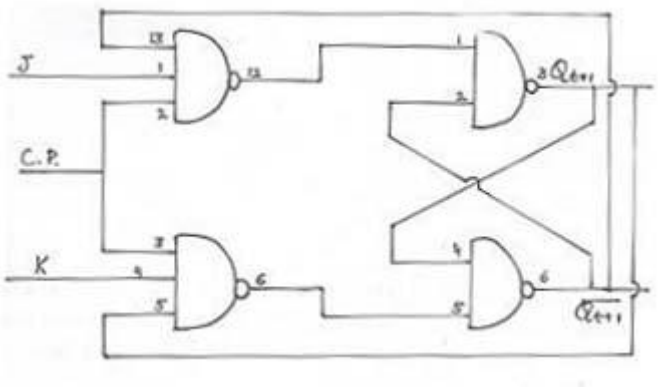
Equipment:

1. 74LS00 x 1
2. 74LS10 x 1
3. EES – 2001 trainer.
4. Cutter.
5. Tweezers
6. Single Core Wires.

Theory:

A J – K flip-flop is a refinement of the RS flip-flop. The indeterminate state of RS flip-flop is defined in J – K flip-flop. The working of J – K flip-flop is identical to that of the RS flip-flop except for one major difference. I.e., J = K = 1 condition does not result in output state, so the flip-flop is not valid. In case of J = K = 1, the J – K flip-flop always goes to its opposite state upon to positive clock transition. This is called “TOGGLE” mode of operation. In this case J and K are both kept high i.e., J = 1 and K = 1 the flip-flop will change states (toggle) for each clock pulse.

Symbolic Diagram:

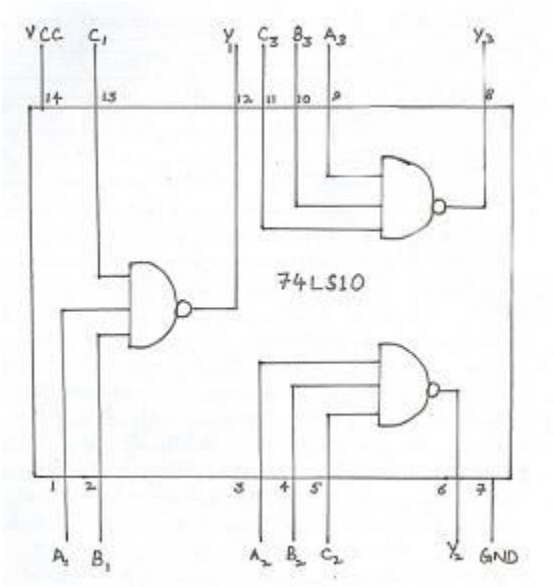


Truth Table:

C.P	J	K	Q_{t+1}	Q_{t+1}'
1	0	1	0	1
1	0	0	0	1
1	1	0	1	0
1	0	0	1	0
1	1	1	TOGGLE	

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.


VCC
C1
Y1
C3
B3
A3
Y3
14
13
12
11
10
9
8
74LS10
1
2
3
4
5
6
7
A1
B1
A2
B2
C2
Y2
GND

Experiment No 14

To check the operation of J – K master slave flip-flop using 74LS00IC and 74LS10IC

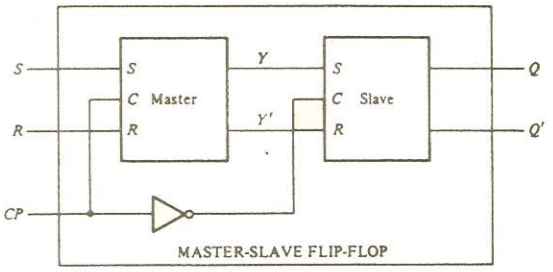
Equipment:

1. 74LS00 x 1
2. 74LS10 x 1
3. EES – 2001 traner.
4. Cutter.
5. Tweezers
6. Single Core Wires.

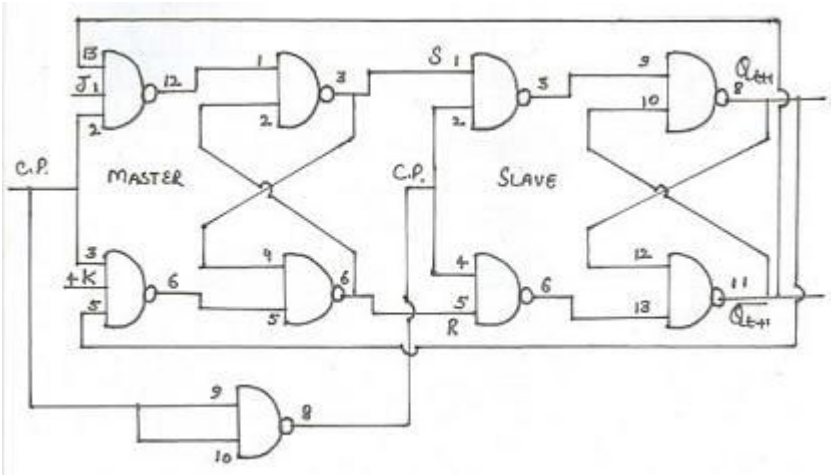
Theory:

A very popular type of J – K flip-flop is master slave (M/S). In (M/S) flip-flop, when C.P = 1, master is enabled and slave is disable. When C.P = 0, Slave is enabled and master is disabled.

Block Diagram:



Symbolic Diagram:



Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 15

To check the operation of register (One pulse parallel transfer) by using NAND IC 74LS00 and IC 74LS76.

Equipment:

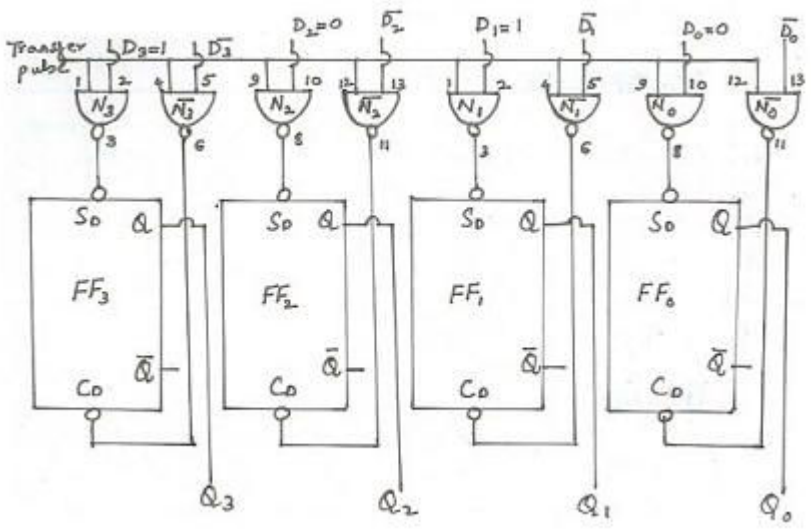
1. 74LS00 x 1
2. 74LS76 x 1
3. EES – 2001 trainer.
4. Cutter.
5. Tweezers
6. Single Core Wies.

Theory:

On-Pulse Parallel Transfer

Parallel transfer can be achieved using the S_D and C_D inputs and a single transfer pulse as shown in Figure. Both the data input bits and their inverse are provided for data transfer into the register. The transfer pulse going high results in selling those stages with input bit 1 and resetting those stages with input bit 0. Before the transfer pulse goes high, the register output data may be different than the input data. When the transfer pulse is high, the output then becomes the same as the input data. Then, when the transfer pulse goes back low, the input gates all go high. Leaving the register holding the transferred data with the input data now free to change (without any affect on the register output).

Symbolic Diagram:



Let, the data to be transferred is; 1010

FF_0 : $D_0 = 0$ $\overline{D_0} = 1$

Output of $N_0 = 1$

$\Rightarrow S_D = 1$

Output of $\overline{N_0} = 0$

$\Rightarrow C_D = 0$

Output of $FF_0 = 0$

FF_1: $D_1 = 1$ $\overline{D_1} = 0$

Output of $N_1 = 0$

$\Rightarrow S_D = 0$

Output of $\overline{N_1} = 1$

$\Rightarrow C_D = 1$

Output of $FF_1 = 1$

FF_2:

$D_2 = 0$ $\overline{D_2} = 1$

Output of $N_2 = 1$

$\Rightarrow S_D = 1$

Output of $\overline{N_2} = 0$

$\Rightarrow C_D = 0$

Output of $FF_2 = 0$

FF_3:

$D_3 = 1$ $\overline{D_3} = 0$

Output of $N_3 = 0$

$\Rightarrow S_D = 0$

Output of $\overline{N_3} = 1$

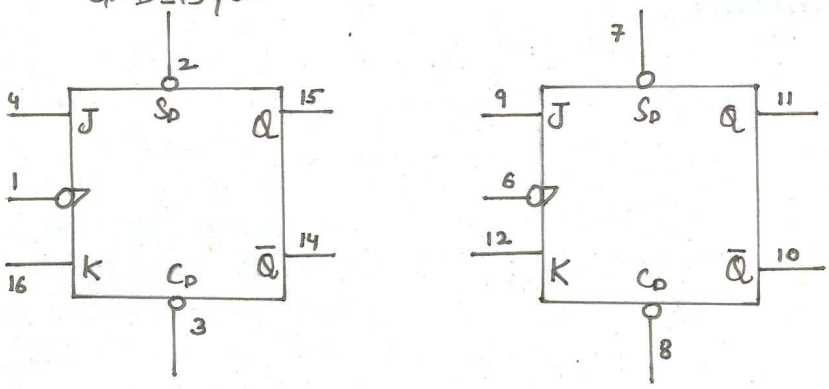
$\Rightarrow C_D = 1$

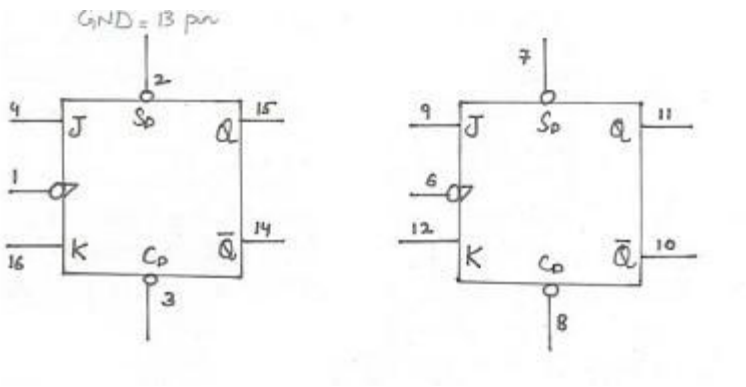
Output of $FF_3 = 1$

PIN BASE CONNECTIONS OF IC 7476

V_{CC}=5 pin

GND=13 pin





Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 16

To check the operation of two stage binary ripple up counter.

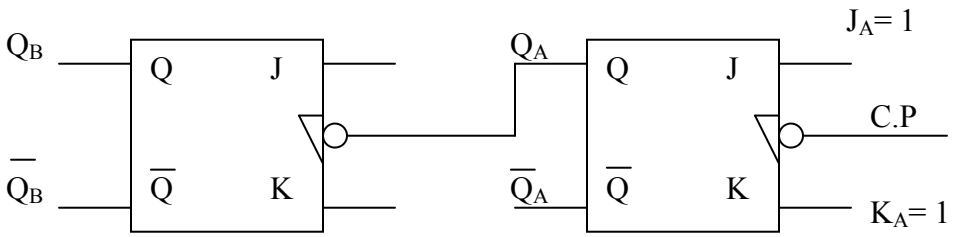
Equipment:

1. 74LS76 x 1
2. EES – 2001 trainer.
3. Cutter.
4. Tweezers
5. Single Core Wires.

Theory:

A sequential circuit that goes through a prescribed sequence of states upon the application of input pulses is called a 'Counter'. A counter that follows the binary sequence is called a 'binary ripple counter'. In two stages binary ripple up counter two J K flip-flops are used. First of all convert JK-ff to T-ff ,that is J=1,K=1.The symbolic diagram is shown below.

Symbolic Diagram:



Truth Table:

Q_B	Q_A	No. of Counts
0	0	0
0	1	1
1	0	2
1	1	3
0	0	4

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 17

To check the operation of three stage binary ripple up counter.

Equipment:

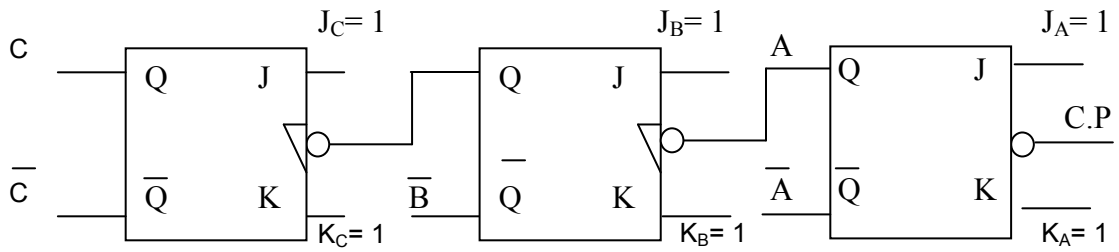
1. 74LS76 x 1
2. EES – 2001 trainer.
3. Cutter.
4. Tweezers
5. Single Core Wires.

Theory:

In three stage binary ripple up counters, three J K flip-flops are used. The J K flip-flops in toggle mode are T- type flip-flops.

In the circuit, the normal output of each flip-flop is connected to the clock pulse of every other (next) flip-flop.

Symbolic Diagram:



Truth Table:

Q_C	Q_B	Q_A	No. of Counts
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	8

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 18

To check the operation of de-multiplexer by using the IC 74LS10 and 74LS04.

Equipment:

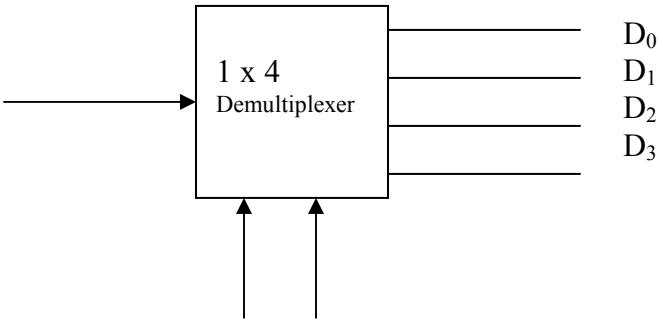
1. 74LS04 x 1
2. 74LS10 x 1
3. EES – 2001 trainer.
4. Cutter.
5. Tweezers
6. Single Core Wires.

Theory:

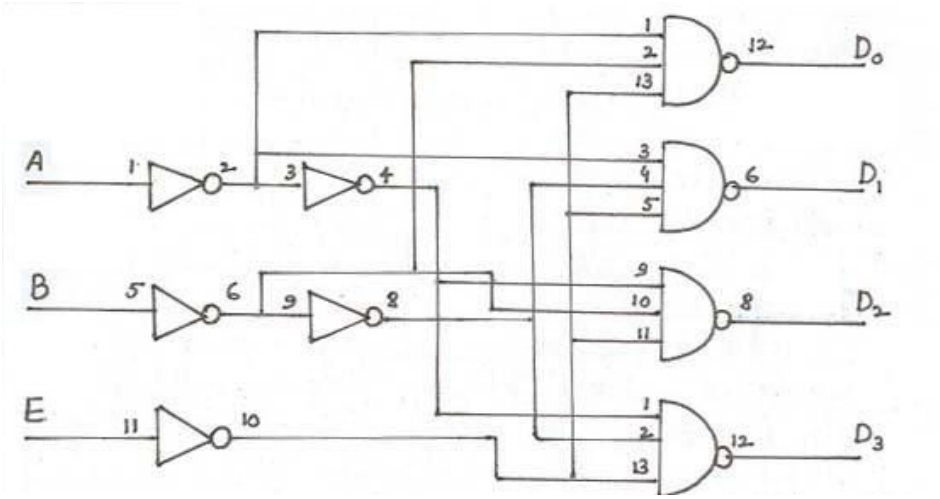
A decoder with an enable input can function as a demultiplexer. A demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines.

All outputs are equal to 1, if enable input is 1. Behaves as a decoder with complemented outputs.

Block Diagram:



Symbolic Diagram:



Truth Table:

Enable	Out Put		Out Put			
E	**A**	**B**	**D_0**	**D_1**	**D_2**	**D_3**
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 19

To construct 2-to-4 line decoder by using 1 – 4 line demultiplexer.

Equipment:

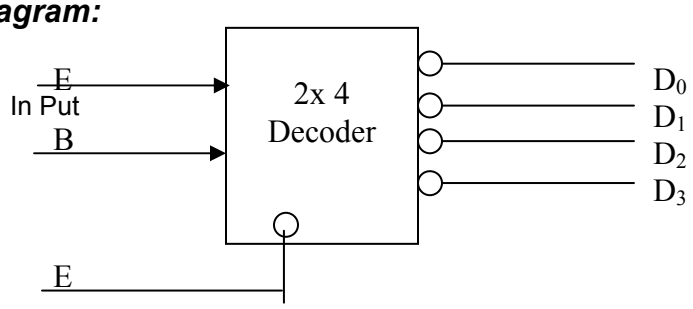
1. 74LS04 x 1
2. 74LS10 x 1
3. EES – 2001 trainer
4. Cutter.
5. Tweezers
6. Single Core Wires.

Theory:

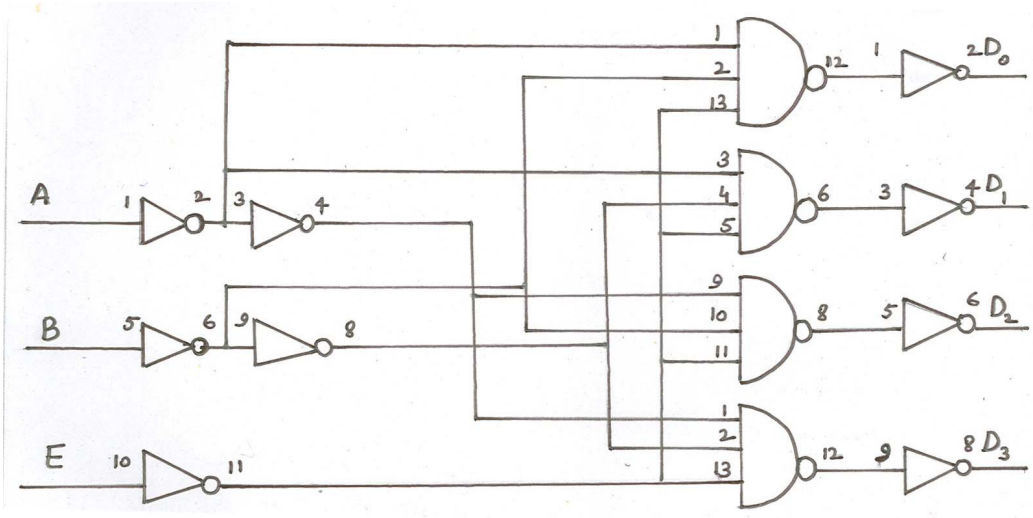
1 – 4 line demultiplexer can form 2 * 4 decoder by placing 74LS04 IC on the outputs of the demultiplexer.

When enable input is 1, then all outputs is zero. When enable input is 0, then the outputs give 1 only at a time, while other outputs are zero. A decoder is a combinational cct. That converts binary information from n inputs to 2^n outputs.

Block Diagram:



Symbolic Diagram:



Truth Table:

Enable	Out Put		Out Put			
E	**A**	**B**	**D_0**	**D_1**	**D_2**	**D_3**
1	X	X	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 20

To check the operation of decoder by using IC 74LS08 and IC 74LS04.

Equipment:

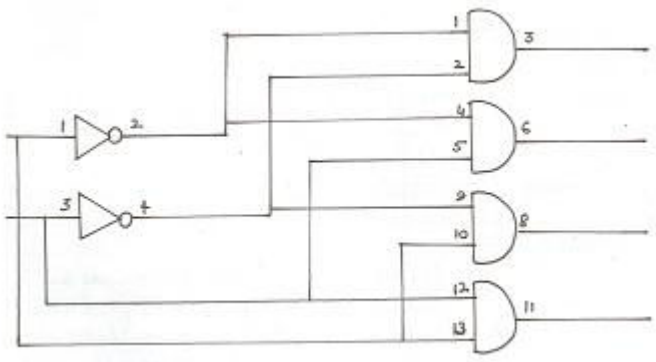
1. 74LS04 x 1
2. 74LS08 x 1
3. EES – 2001 trainer.
4. Cutter.
5. Tweezers
6. Single Core Wires.

Theory:

A decoder is a combinational circuit that converts binary information from n inputs to 2^n outputs.

The outputs of a decoder gives one 1 at only one time while they give zero 0 for rest. In the truth table, the 1's of outputs are present in diagonal position.

Symbolic Diagram:



Truth Table:

In Put		Out Put			
A	**B**	**D_0**	**D_1**	**D_2**	**D_3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.

Experiment No 21

To check the operation of multiplexer by using IC 74LS04, IC 74LS08 and IC 74LS32.

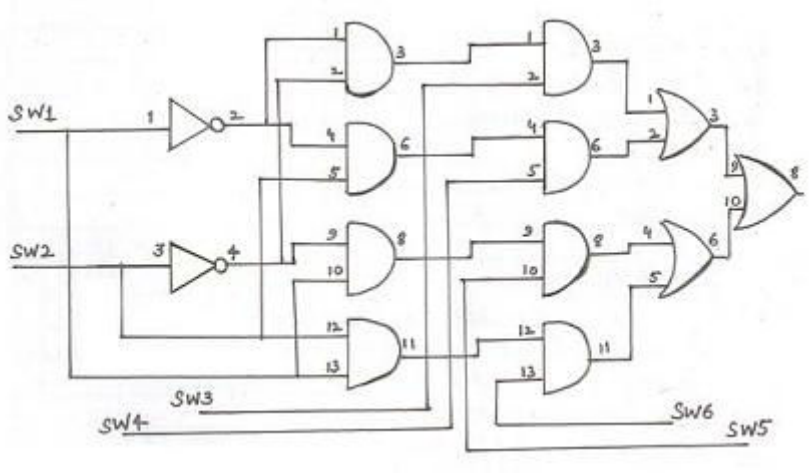
Equipment:

1. 74LS08 x 1
2. 74LS04 x 1
3. 74LS32 x 1
4. EES – 2001 trainer
5. Cutter.
6. Tweezers
7. Single Core Wires.

Theory:

Multiplexing means transmitting a large number of information units over a smaller number of channels or lines.a digital multiplexer is a combinational circuit that selects binary information from one of many input lines and direct it to a single output line,there are 2n inputs lines and n selections lines whose bit combinations determine which input is selected.A4-to –1line multiplexer is shown in the following fig. There are two selection lines and four input lines selection lines selects particular line.

Symbolic Diagram:



Truth Table:

Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	L1
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	0
0	1	0	1	0	0	1
1	0	0	0	0	0	0
1	0	0	0	1	0	1
1	1	0	0	0	0	0
1	1	0	0	0	1	1

Precautions:

1. The connections should be clean and tight.
2. The power supply should be checked.