Conductor supports a generous flow of when a voltage is applied across it eg copper, aluminium

Insulator is that offers very low conduction (flow of charges) when voltage is applied eg mica → used for thermal and electrical wood.

Semiconductors conductivity is more than but less than conductors. eg silicon and germanium

Resistivity = $\frac{1}{\text{conductivity}}$ $\rho = \frac{1}{\sigma}$

fixed for every material

If resistivity is high → current is low.

For conductors (copper) $\rho = 10^{-6}$ Ω-m

Insulators (mica) $\rho = 10^{12}$ Ω-cm

For silicon $\rho = 500 \times 10^{3}$ Ω-cm

Germanium $\rho = 50$ Ω-cm

$\rho_c < \rho_s < \rho_i$

$I_c > I_s > I_i$

Energy Band Diagram

In general atom is present in l
So in lattice one atom will
influence on the shell of
atom. so the outermost
will split into valence band
the conduction band.

Electrons present in conduction band
participate in conduction.

conduction band

If electron is present in valence band, we have to transfer it to the conduction band.

How ?

By giving energy equal to the band gap or forbidden gap → no stays here. (E_0 or E_g).

Band gap = High so more energy required transfer electrons. → Therefore not good conductor.

$E_0 = 6\ eV$ $(1\ eV = 1.6 \times 10^{-19}\ J)$

Semiconductor

Germanium = 0.75 eV
Silicon = 1.16 eV

$E_0 = 1\ eV$ Ge < Si

Germanium → more no. of orbits → force of attraction b/w valence electrons and nucleus is smaller.

→ less no. of orbits → strong attractive force.

Conductor

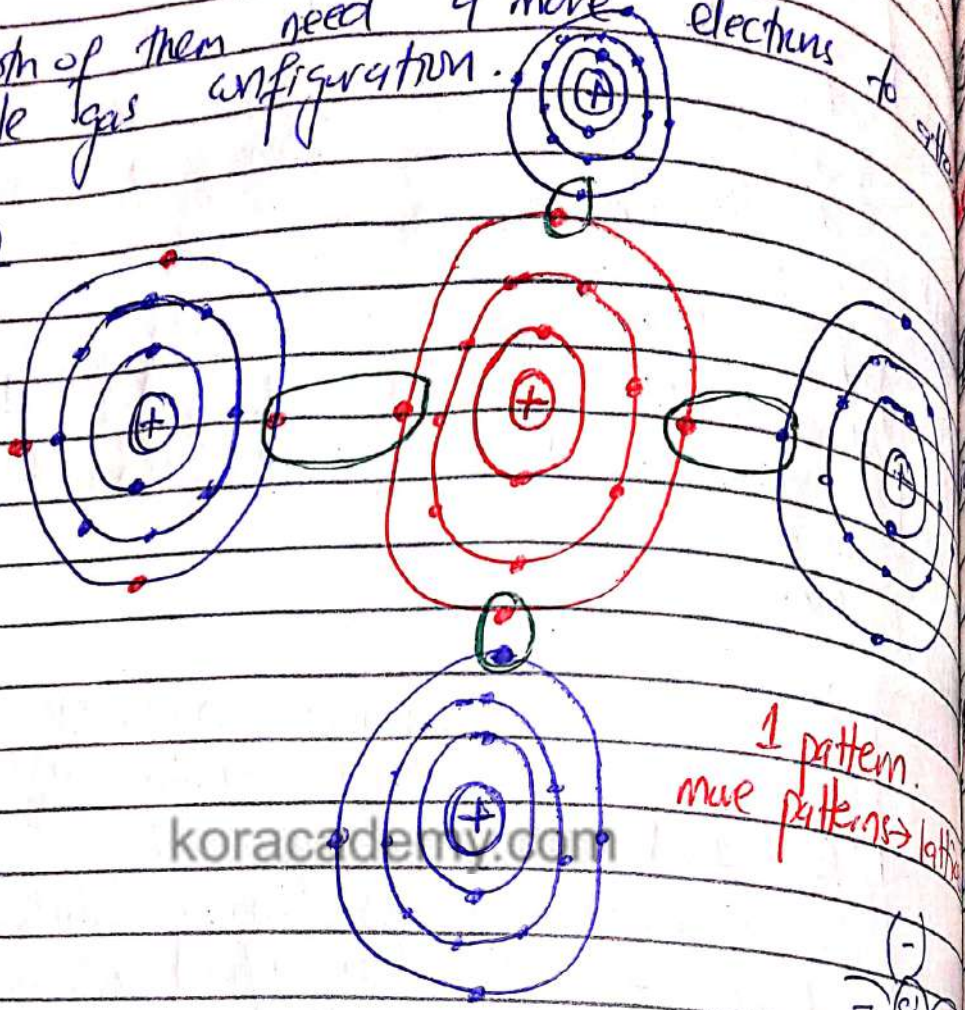
overlapping conduction and valence band → no forbidden gap.

Electron is free to move from valence to conduction band without giving any external energy.

Group IV of periodic table
Si → atomic number = 14 → 2, 8, (4)
Germanium → at no = 32 → 2, 8, 18, (4)

Both of them need 4 more electrons to attain noble gas configuration.

Silicon



1 pattern.
more patterns → lattice

Instinsic And Extrinsic semiconductors

Instrinsic are pure semiconductors.
(no other atom present eg silicon lattice

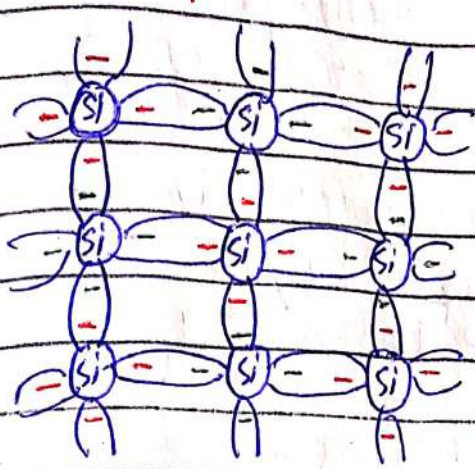
Free electrons are ally due to natural causes.
(light thermal energy) → electrons in cov
bond will obtain the kinetic energy, brea
the bond and will be available for cond

Increase of Temp ∝ No. of free electrons.

temp ∝ 1/resistance for -ve temp coefficient.

silicon and germanium both have -ve temp cft.

Conductors (metals) have +ve temp coefficient.
Increase of temp ∝ Resistance.



lattice

Intrinsic

Impurity atoms are also added.

types of impurities are present:

Pentavalent atoms of group V → V valence
electrons antimony, phosphorus, arsenic. etc

Trivalent atoms of group III eg boron,
gallium, Al, Indium.

we add impurity atoms to intrinsic semiconductors
(e) to make extrinsic.

at what proportion?

Add 1 part in 10 million means in 10
million atoms of intrinsic S.C we add 1
impurity atom.

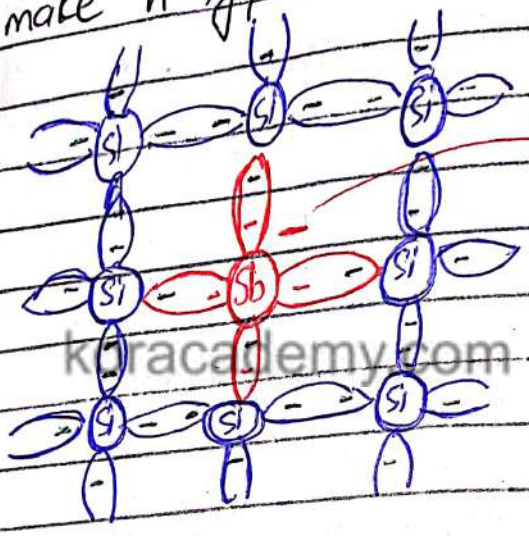
adding of impurity will change the electrical
properties of intrinsic S.C.

Process of adding certain impurity to pure semiconductor is called DOPING

Because of doping we have two types of extrinsic semiconductors

(i) n type Pentavalent impurity is added
(ii) p type trivalent impurity is added.

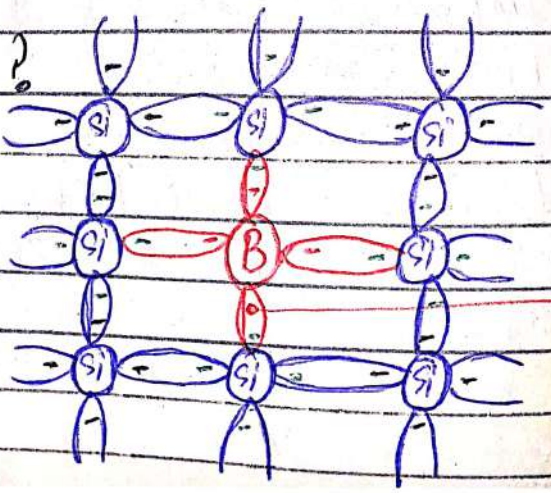
How to make n type semiconductor?



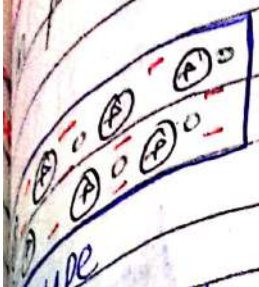
If potential difference is applied across material. Then this free electron will be drifted and we have electron current.

In n type, we have electron as charge carriers.

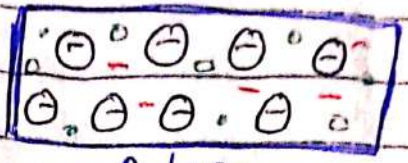
For P type?



P type, we have holes as charge carriers.



P type



P type.

- immobile ions
- majority charge carriers
- minority charge carriers

• → majority charge carriers.
— → minority charge carriers
⊖ → boron atom will get electron from neighbouring to be negatively charged.

Electron Vs Hole Flow

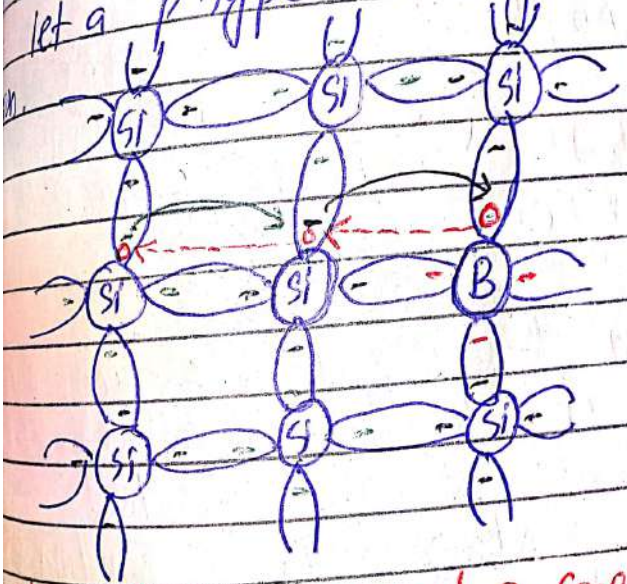
type of charge carriers.

ion of current is opposite to the direction of of electron

$\bar{e}$ → then I ← conventional current.

onal current ⇒ $\bar{e}$ → I →

let a P type ie. eg silicon dopped with

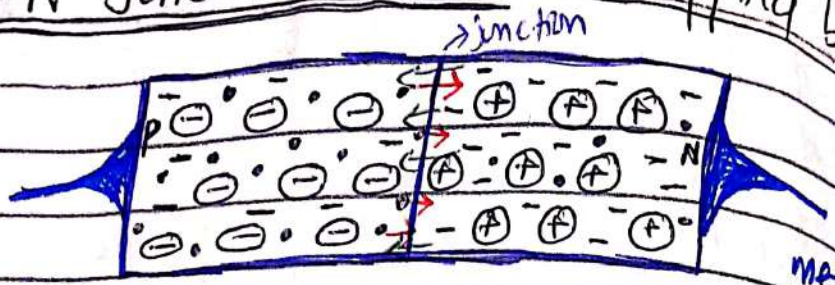


The neighboring atom will provide electron to boron and this way the movement of the hole will occur.

ection of hole movement is same as direction of current.

the charge on the donor atom and H
moving → conventional current

P-N Junction Diode (No applied bias)



Bias

Application of external voltage across two terminals.

BJT → Bipolar junction transistor. ⇒ 3 terminal device.

	majority	minority
P type	Holes	Electrons } Due to exp
n type	Electrons	Holes } because electron gain energy and break covalent bond and does not depend on external voltage applied.

Diffusion or Ion implantation → processes to consume N and P type → dope one side with Pentavalent and the other with trivalent impurities.

More holes on the P side so they will move towards N side and similarly electron will move from N to P side.

⇒ movement of charge through junction ⇒ current

This movement of charge carriers from high to low concentration is called diffusion and

is called diffusion current. → due to charge carriers.

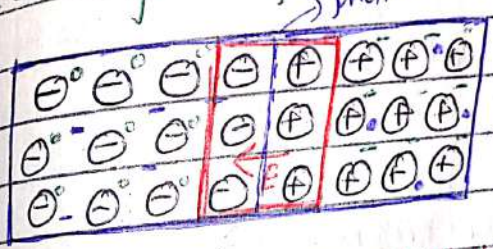
depletion layer?

because of diffusion holes from P side combines with electrons on N side and in same way electrons from N side combine holes from P side and as the combination takes place immobile ions will surface out because of diffusion.

surface out? Uncovering of immobile ions.

ions have holes ⊕ ions have electrons electrical neutrality is maintained. as holes are combining with electrons we only left with +ve and -ve ions

depletion region there are no mobile charges only uncovered immobile ions. we call it depletion region because it is depleted of free carriers.



electric field in the depletion region. → also called as the space charge region. there now no movement of charges. This potential is acting as barrier to the further movement of holes and electrons. ⇒ barrier potential / built in potential. electrons to right - Holes to left ⇒ Drift current

has direction opposite to diffusion current

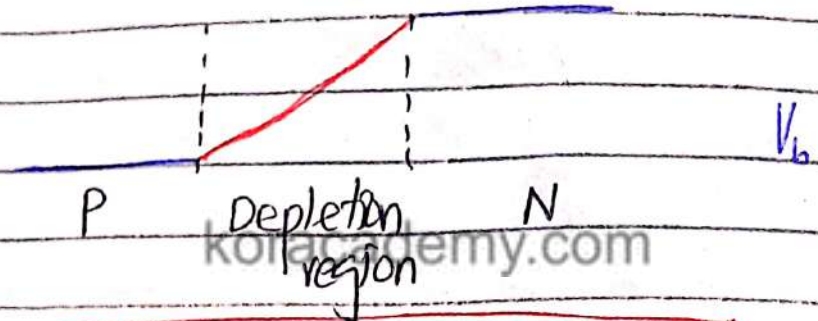
Under steady state, diffusion and drift currents are equal.

Drift current is due to minority charge carrier

Net current = 0 for open circuit P-N junction diode.

$O^{o} + e \rightarrow \ominus$

$O^{e} + o \rightarrow \oplus$ in depletion layer.



$$V_b = \frac{KT}{e} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$V_T = \frac{KT}{e}$ ⇒ thermal voltage = voltage equivalent of temperature.

K = Boltzmann's constant = 1.38066×10^{-23} J

T = absolute temp (K)

e → charge of electron = 1.6×10^{-19} C

N_A → Acceptor concentration

N_D → Donor concentration

n_i → Intrinsic carrier density

V_T at room temperature = 0.026 volts

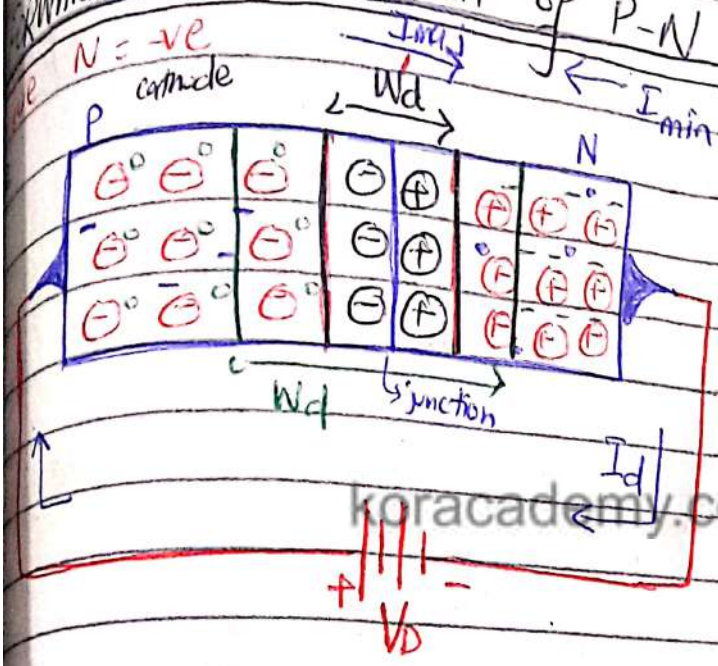
width of depletion region

$$W_d = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$$

silicon $\varepsilon = 1.04 \times 10^{-12}$ F/cm.

germanium $\varepsilon = 1.12448 \times 10^{-12}$ F/cm

FORWARD BIAS condition of P-N junction diode



if $V_d = 0 \Rightarrow W_d$

$V_d > 0 \Rightarrow W_d'$

$W_d' < W_d$

$V_D \propto \frac{1}{W_d}$

Because of the +ve terminal the holes will be repelled towards the depletion region and similarly the -ve terminal will repel the electrons towards depletion layer b/c electrons are +vely charged.

Thus the forward bias potential V_D will depressive the electrons on N side and holes on P side to recombine with the ions near the boundary and reduce the width of depletion region

$I_D = I_{maj/diffusion} - I_{minority}$

Rise of temp $\propto$ No. of minority carriers

Hence the no. of minority charge carrier will be the same under forward bias condition.

Barrier potential is also reducing in forward

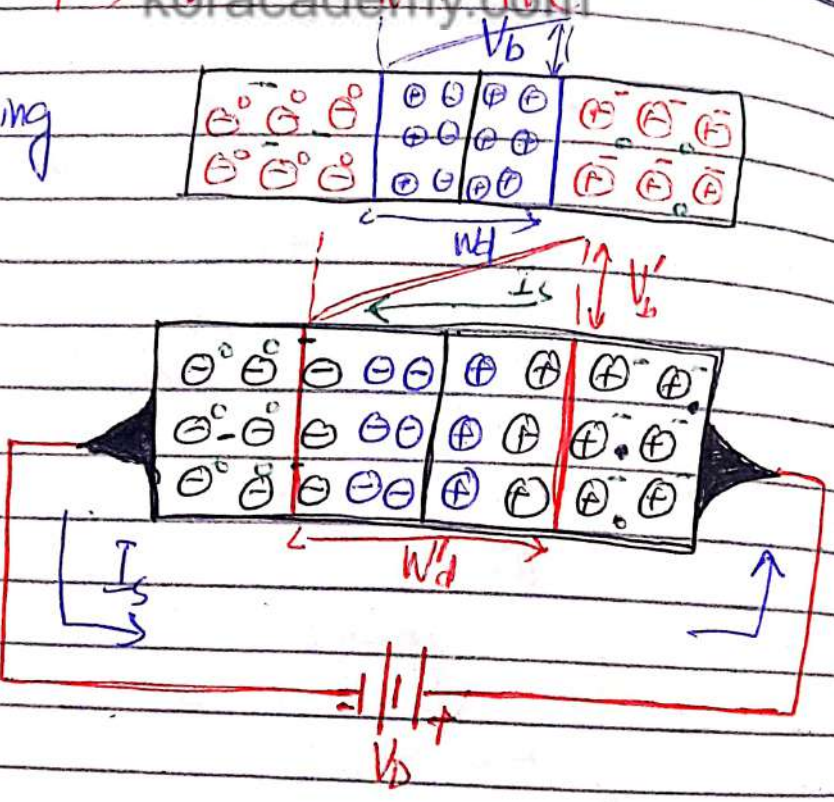
New Barrier potential = $V_b - V_D$
↳ previous B. P under

Once the barrier potential is zero the flow of electrons will pass through the junction the current rises exponentially

Reverse saturation current → current due to minority carriers remains the same.

REVERSE BIAS condition of PN junction diode

P → -ve N → +ve



Attraction b/w holes and -ve terminal and electrons of N side and +ve terminal.
So uncovering of immobile ions take place.

$V_b' = V_b + V_d$

$V_d \propto V_b'$ $\quad V_d \propto W_d'$

$W_{d(rb)} > W_{d(nb)} > W_{d(fb)}$

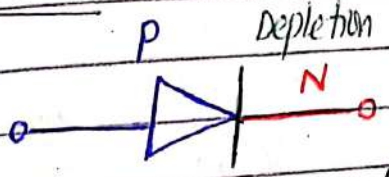
$V_{b(rb)} > V_{b(nb)} > V_{b(fb)}$

The majority charge carriers cannot overcome the increased barrier potential (as width of depletion region has increased and now also the barrier potential) $I_{maj} \approx 0$

No. of minority charge carriers will not change and hence minority carrier flow will remain same as no applied bias.

So under reverse bias only one current exists ie the reverse saturation current I_s → very small (μA).

Symbol of diode



Diode current voltage relation

$$I_D = I_s \left(e^{\frac{KV_D}{T}} - 1 \right)$$

I_D → diode current V_d → voltage across diode

I_s → reverse saturation current $K = 11600/\eta$

η → ideality factor. → ranges b/w 1 and 2

{ $\eta = 1$ for Ge $\eta = 2$ for Si } → both

For high $I_d \Rightarrow \eta = 1$ for both Si and

As $K = \frac{11600}{\eta} \Rightarrow K\eta = 11600$

Also $V_T = \frac{T_K}{11600} \Rightarrow V_T = \frac{T}{K\eta}$

So $\frac{K}{T_K} = \frac{1}{V_T \eta}$

$$I_D = I_S \left(e^{\frac{V_D}{\eta V_T}} - 1 \right)$$

eg A germanium diode displays a forward voltage of 0.25 V at 10 mA current. room temperature. Find the reverse saturation current.

$V_D = 0.25\ V \qquad I_D = 10 \times 10^{-3}\ A$

$T = 27° + 273 = 300\ K$

$$V_T = \frac{T}{11600} = \frac{300}{11600} = 0.026\ V$$

$I_S = ?$

$$I_D = I_S \left(e^{\frac{V_D}{\eta V_T}} - 1 \right)$$

$\eta = 1$ Putting values and solving

$I_S = 6.67 \times 10^{-9}\ mA$

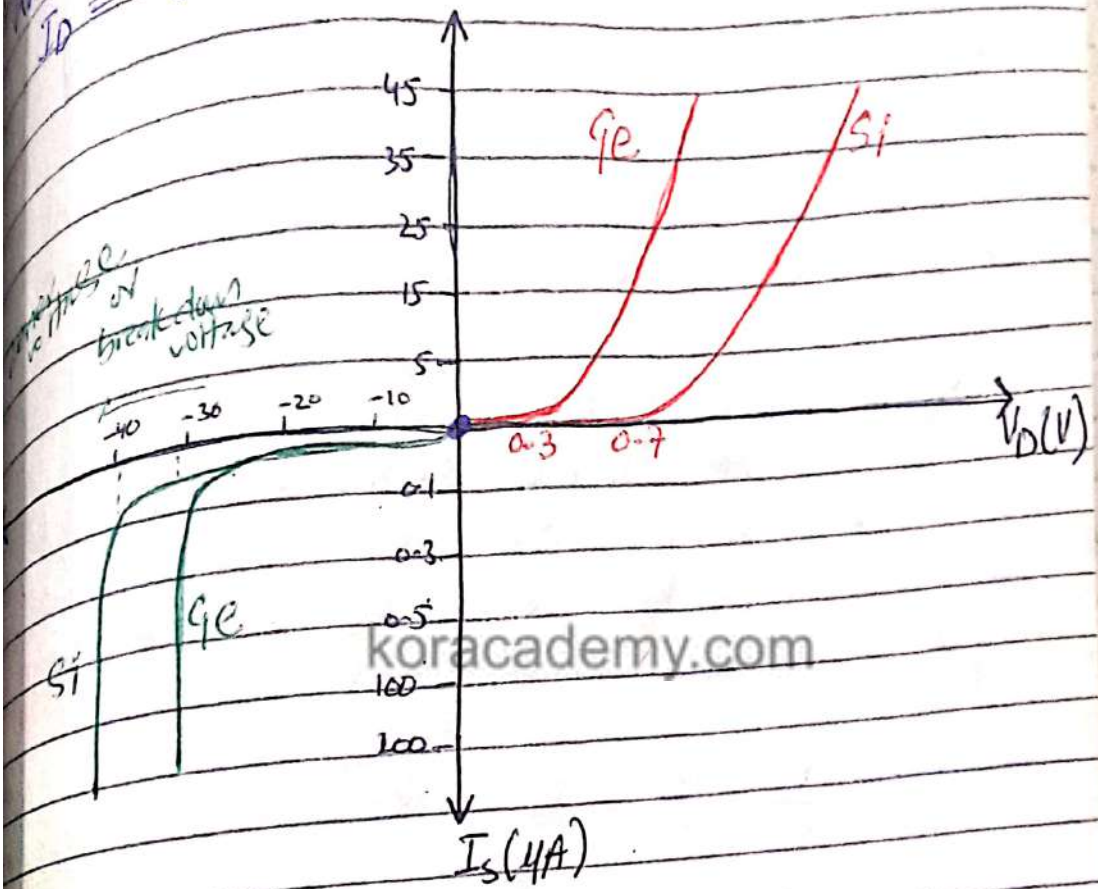
or $I_S = 6.67 \times 10^{-7}\ A$

Characteristics of P-N junction Diode

$$I_D = I_S\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

When $V_D = 0$ (no applied bias)

$I_D = I_S(e^0 - 1) \Rightarrow I_D = 0$



ward bias

↑ W_d ↓ V_b ↓

when $V_d = V_b$ → flood of electrons crossing junction and we have rapid increase current.

Germanium $V_b = 0.3$ V Silicon $V_b = 0.7$ V

everse bias

$V_D < 0$

$I_D = I_S\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$

I_S → also called leakage current

$I_D \simeq I_S$ ($I_{maj} \simeq 0$)

Called breakdown voltage because at voltage breakdown of diode occurs Breakdown?

On increasing reverse bias voltage to a very high value the electrons will acquire a very high kinetic energy they will break the covalent bond and become free. These free electrons will collide with more electrons and make them free too. This process will continue like a chain reaction.

Peak Inverse Voltage (PIV)

The maximum reverse bias voltage that can be applied across the diode before entering the zener or breakdown region.

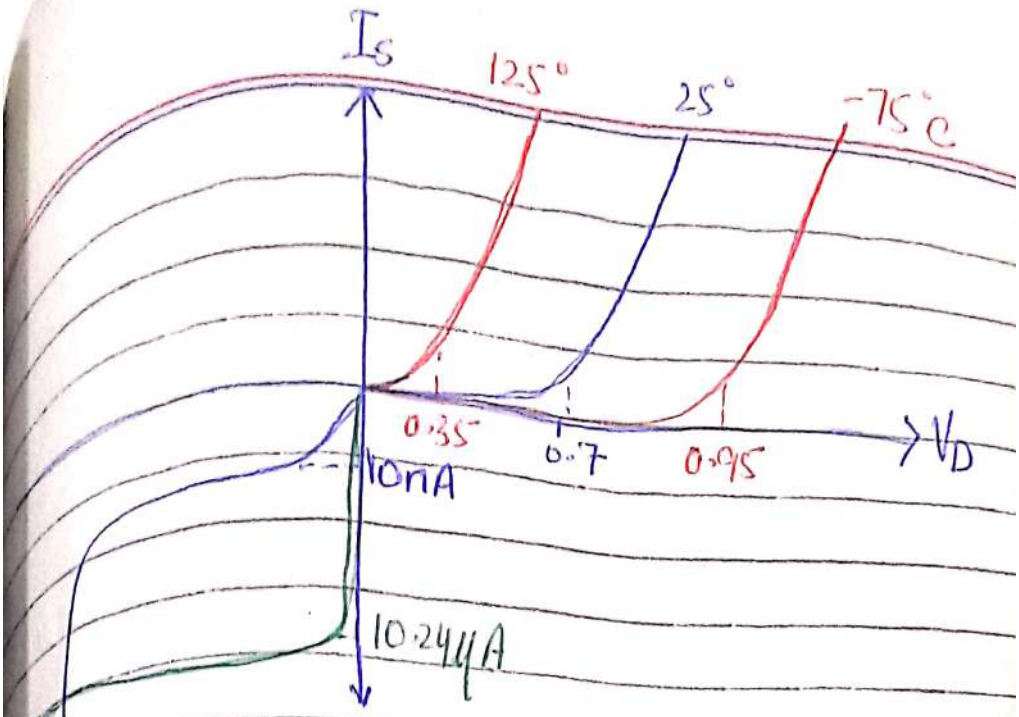
Effect of temperature on VI characteristics

In forward Bias the characteristics of silicon diode shift to the left at a rate of 2.5 mV per degree °C rise in temperature

On decreasing shift to right.

In ~~forward~~ Reverse bias the reverse saturation current (I_s) doubles for every 10°C rise in temperature.

It should be closer to 10pA for high temperature applications.



at 25°C ⇒ $V_D = 0.7$ V

for 100°C rise in temp at 125°C

$100 \times 2.5mV = 0.25$ V.

V_D will reduce by 0.25 V.

New $V_D = 0.7 - 0.25 = 0.35$ V.

for 100° drop in temp ie at -75°C.

100×2.5 mV = 0.25

New $V_D = 0.7 + 0.25 = 0.95$

Zener potential increases when we decrease temperature and Zener potential decreases when we increase the temperature.

for 100°C rise in temp at 125°C.

25°C → 10nA ⇒ 35°C → 20nA ⇒ 45°C → 40nA

55°C → 80nA ⇒ 65°C → 160nA ⇒ 75°C → 320nA

85°C ⇒ 640 ⇒ 95°C → 1280nA ⇒ 105°C → 2560

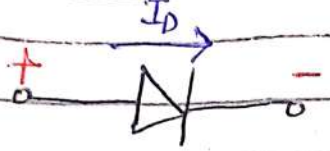
115°C → 5120. ⇒ 125°C → 10240nA or 10.24μA

Germanium has high saturation current so less applications and use cases for silicon and gallium arsenide.

most popular

Ideal Vs Practical Diode

Forward Bias



Generates flow of current.

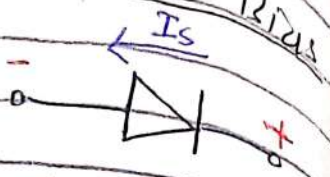
$I_D = I_{maj} - I_S$

Diode resistance $r_D \rightarrow$ Very small

$r_D = 0$ → for ideal diode

Acts as closed mechanical switch

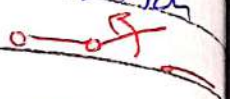
Reverse Bias



Very small current

$I_S \simeq 0$ $r_D \simeq \infty$

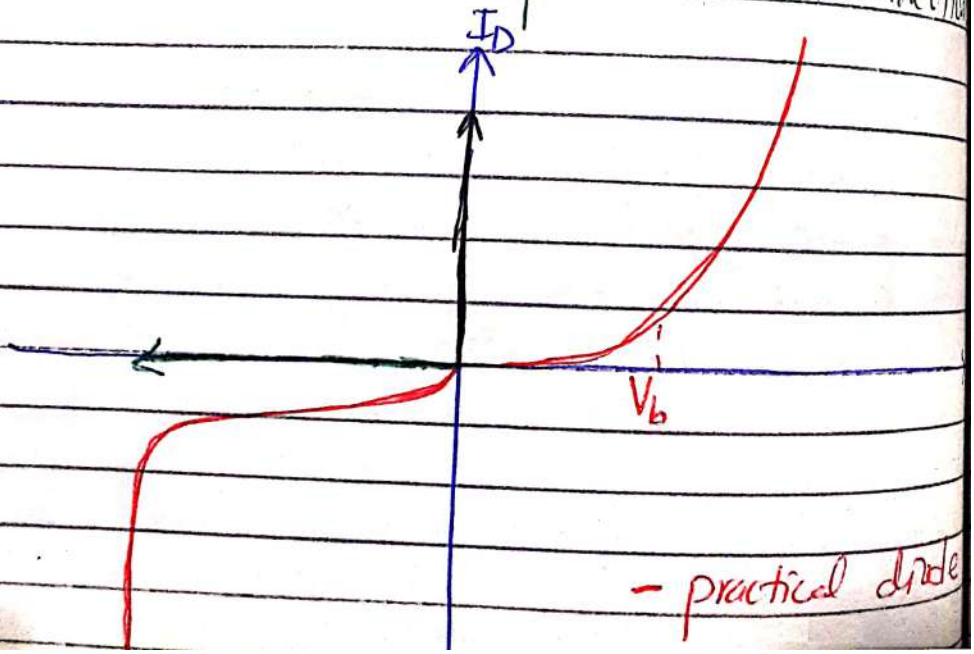
Acts as open mechanical switch



$r_D \rightarrow$ Very large

→ practical diode

Semiconductor diode only permits the current flow in one direction whereas in mechanical switch, current can flow in both directions



– practical diode

$V_D = I_D r_D \Rightarrow V_D = 0$

$r_p = 0$ sign ideal diode

$V_D = I_D r_D \Rightarrow I_D = \infty$

le Equivalent Circuits

valent Circuits ?

An equivalent circuit is a combination elements (like R, C, L) properly chosen best represent the actual characteristics device in a particular operating region

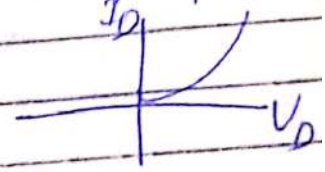
iece wise linear equivalent circuit

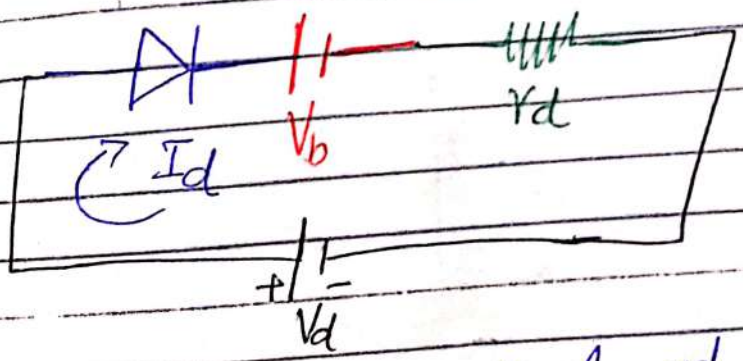
ve will assume the curve to be linear with small non linearity.

$r_D = \frac{1}{\text{slope}}$ slope $= \tan\theta$ $\tan\theta = P/B$

$r_e = I_D / V_D$ $V_D = I_D r_D \Rightarrow r_D = V_D / I_D$

$r_{slope} = V_D / I_D = r_D$





t at 0.8V the $I_D = 10mA$ and we have find r_D. $r_d = \frac{(0.8 - 0.7)}{(10 - 0) \times 10^{-3}}$

$r_D = 10\Omega$

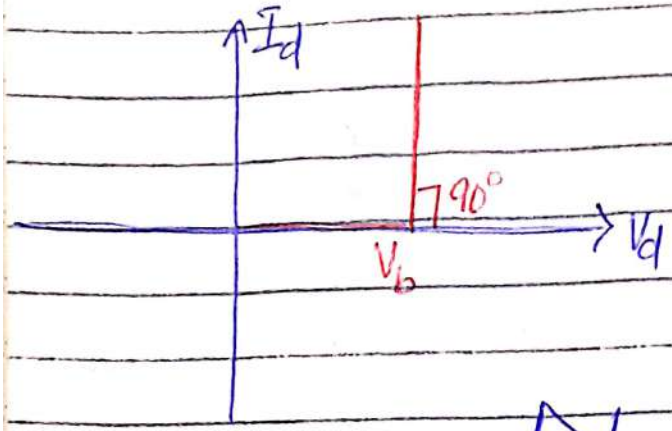
(ii) Constant voltage Drop / Simplified ckt

Two assumptions:

(i) Consider linear one ignoring small non-linear

(ii) Consider $V_D = 0 \Rightarrow \frac{1}{\text{slope}} = 0 \Rightarrow$ slope $= \infty$

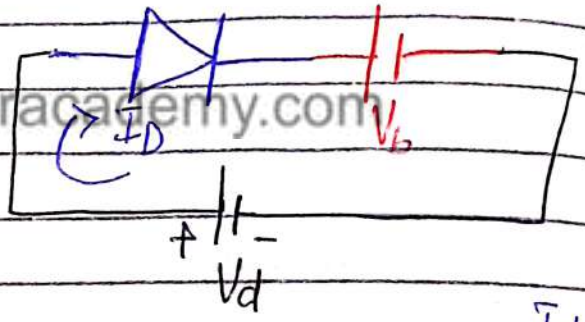
$\Rightarrow \tan\theta = \infty \quad \theta = \tan^{-1}(\infty) \Rightarrow \theta = 90°$



(mostly used)

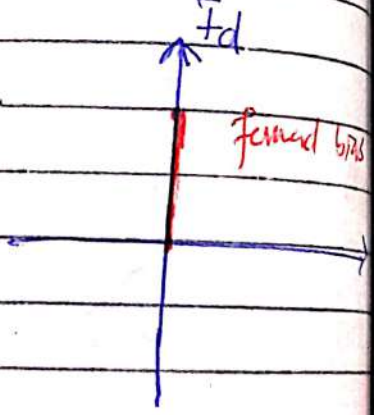
$V_d \geq V_b$ ——

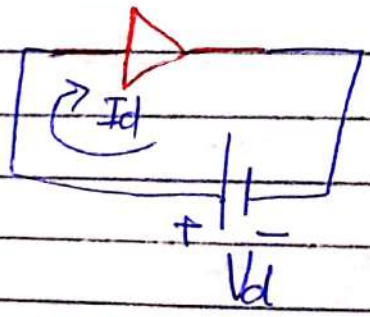
$V_d < V_b$ ---



(iii) Ideal equivalent Circuit

$V_D = 0 \quad V_b = 0$





5V —▷|— 0V

replace diode by its battery potential

eg 5V —|— 0V

0.7V

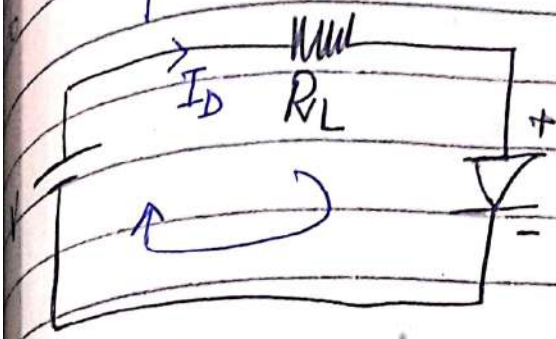
(if 1.5V)

Reverse bias: 0V ——▷|—— 5V

no current so "open circuit"

Load Line Analysis of Diode

used for non linear electric circuits. → That not follow ohm's law.



Apply KVL

$V - I_D R_L - V_D = 0$

OR

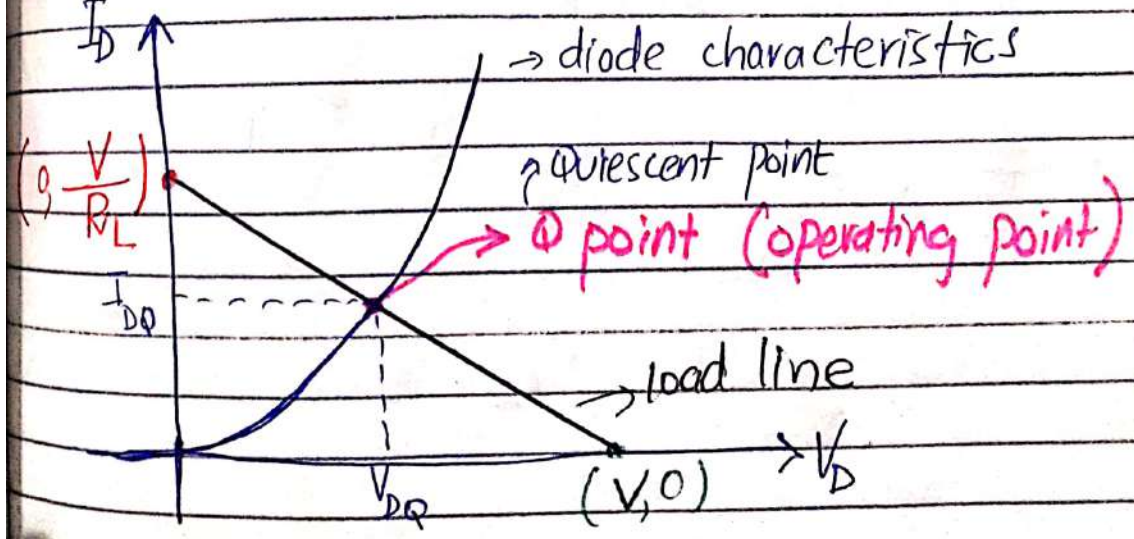
$$V = I_D R_L + V_D \rightarrow (1)$$

When $V_D = 0$

$(1) \Rightarrow V = I_D R_L \Rightarrow \boxed{I_D = \frac{V}{R_L}}$

When $I_D = 0$

$(1) \Rightarrow \boxed{V = V_D}$



Slope of load line?

① $\Rightarrow V = I_D R_L + V_D$

$$\frac{V}{R_L} = \frac{I_D}{} + \frac{V_D}{R_L}$$

$$\Rightarrow I_D = \frac{V}{R_L} - \frac{V_D}{R_L}$$

As line equation $y = mx + c$

& rearranging $I_D = -\frac{V_D}{R_L} + \frac{V}{R_L}$

$c = \frac{V}{R_L}$ slope $(m) = \frac{-1}{R_L}$

$I_D = y$ $V_D = x$

So by changing R_L, the Q point will also change because slope will change

Q. Determine the Q point and V_R (voltage drop across resistor).

$V_\gamma = 0.8$ (graph)

$V = 10V$ $R_L = 1k\Omega$

KVL $10 - 10^3 I_D - V_D = 0$

$10 = 1 \times 10^3 I_D + V_D$

I_D when $V_D = 0$

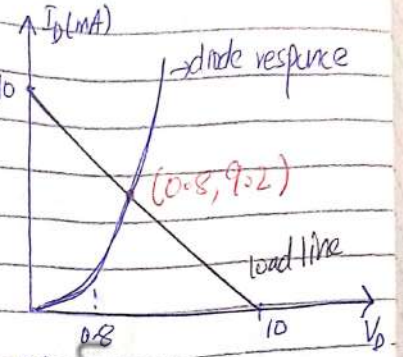
$10 = 10^3 I_D$

$\Rightarrow I_D = 10mA$

When $I_D = 0$

$10 = 10^3 (0) + V_D$

$\Rightarrow V_D = 10$



$(0.8, 9.2)$

ohm's law

$V_R = I_D R_L$

$= (9.2 \times 10^{-3})(1 \times 10^3)$

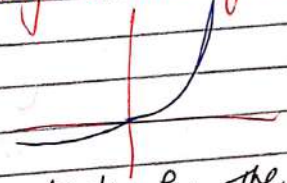
$\Rightarrow V_R = 9.2$ volts.

le Resistance Levels (DC Resistance) ①

s the operating point of diode moves, stance of diode will also change.

hen we apply a DC voltage to a circuit ng semiconductor diode, the operating t will not change with time because d V_{DQ} will not change in case of DC.

$$R_D = \frac{V_{DQ}}{I_{DQ}}$$

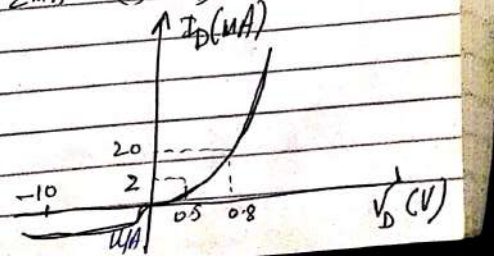


Determine the dc resistance levels for the de at (a) $I_D = 2$mA (b) $I_D = 20$mA

$V_D = -10$V

$R_D = \frac{V_D}{I_D} = \frac{0.8}{20 \times 10^{-3}}$

$\Rightarrow R_D = 40\Omega$



(a) $R_D = \frac{0.5}{2 \times 10^{-3}} \Rightarrow R_D = 250\ \Omega$

(c) $R_D = \frac{10}{1 \times 10^{-6}} \Rightarrow R_D = 10\ M\Omega$

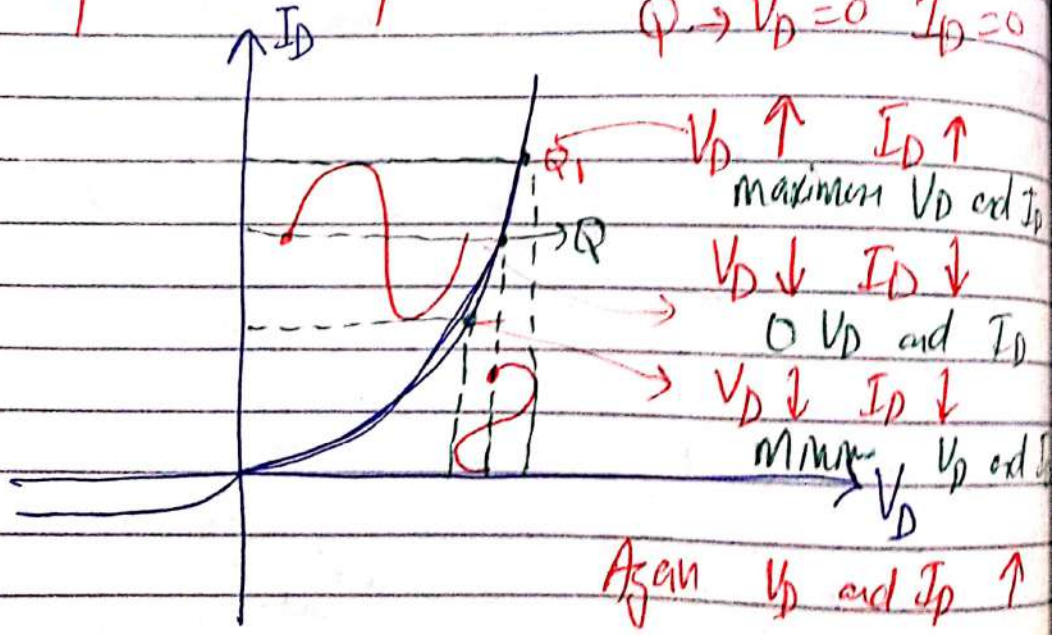
$c < a < b$ Currents

$c > a > b$ Resistance

② AC Resistance

When we apply an AC input in place of DC, the input will vary and will move the instantaneous operating point up and down.

In DC input $R_D = \frac{V_D}{I_D}$ we cannot this equation for AC input.



Q → $V_D = 0$ $I_D = 0$

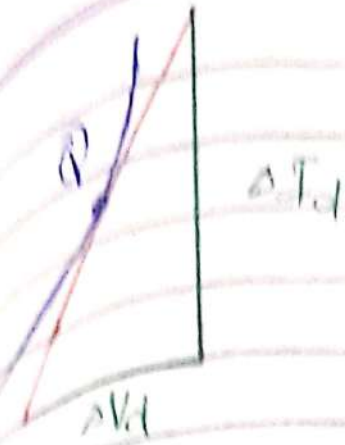
$V_D \uparrow$ $I_D \uparrow$ maximum V_D and I_D

$V_D \downarrow$ $I_D \downarrow$ 0 V_D and I_D

$V_D \downarrow$ $I_D \downarrow$ minimum V_D and I_D

Again V_D and I_D ↑

Redrawing the region of Q point.



tangent through Q point

$$r_d = \frac{\Delta I_d}{\Delta V_d}$$

$$r_d \propto \frac{1}{\text{slope}}$$

numerical problems we will use;

$$r_d = \frac{26mV}{I_d}$$

diode current $I_D = I_S(e^{V_D/\eta V_T} - 1)$

$$I_D = I_S e^{V_D/\eta V_T} - I_S \rightarrow (1)$$

$$\frac{dI_D}{dV_D} = I_S \frac{d}{dV_D}(e^{V_D/\eta V_T}) - \frac{d}{dV_D}(I_S)$$

(I_S → constant → 0)

As $\frac{d}{dx} e^{ax} = a e^{ax}$

$$\Rightarrow \frac{dI_D}{dV_D} = \frac{I_S}{\eta V_T} e^{V_D/\eta V_T}$$

$I_D + I_S$

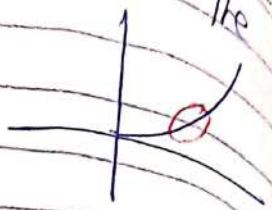
As $I_D >> I_S$ $\quad I_S \downarrow 0$

$$\Rightarrow \frac{dI_D}{dV_D} = \frac{I_D}{\eta V_T} \quad \text{or} \quad \frac{dV_D}{dI_D} = \frac{\eta V_T}{I_D}$$

If $\eta = 1$ $\quad V_T = 26mV$

$$\Rightarrow r_d = \frac{dV_D}{dI_D} = \frac{26mV}{I_D}$$

When I_D is small, $\eta \neq 1$, $\eta = 2$
This equation is not valid near the knee



③ Average AC Resistance

When input voltage is large, it produces a broad swing in the characteristics and the resistance in this region is known as average AC resistance.

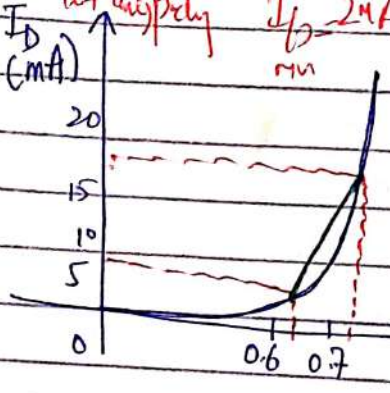
The average AC resistance is the resistance determined by a straight line drawn between the two intersections obtained by the maximum and minimum values of input voltage.

$$r_{av} = \frac{\Delta V_d}{\Delta I_d}$$ | point to point

let $V_{min} = 0.650V$ and $V_{max} = 0.725\ V$

$I_{D_{min}} = 2mA$ (given)

$I_{D_{max}} = 17\ mA$



$$r_{av} = \frac{0.725 - 0.650}{17mA - 2mA}$$

$$r_{av} = \frac{0.075}{15\ mA}$$

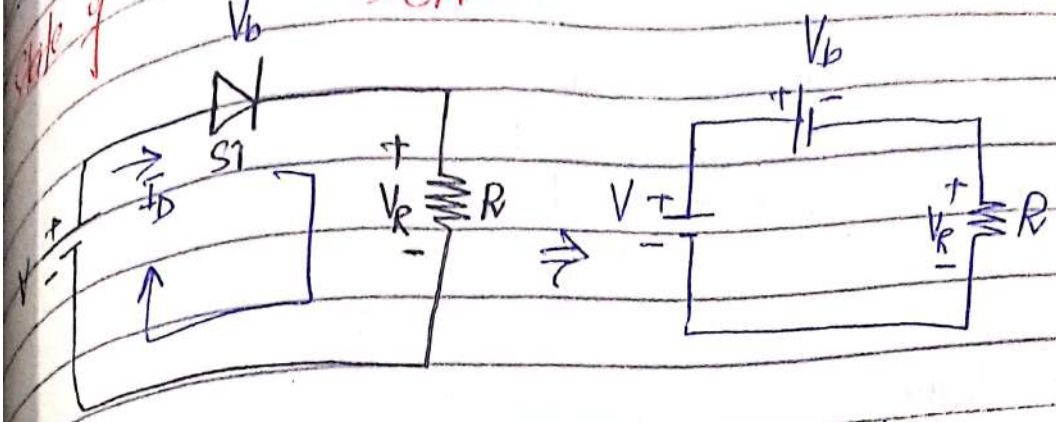
$$\Rightarrow r_{av} = 5\Omega$$

$r_d|_{V_D = 0.65} \Rightarrow 5\Omega$

$r_d|_{V_d = 0.725} < 5\Omega$

Series Diode Configurations

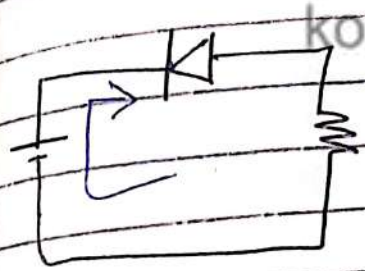
State of diode → ON (with the direction of current with arrow of the diode.)
→ OFF



KVL $V - V_b - V_R = 0$ or $V_R = V - V_b$

$I_D = I_R = V_R / R$

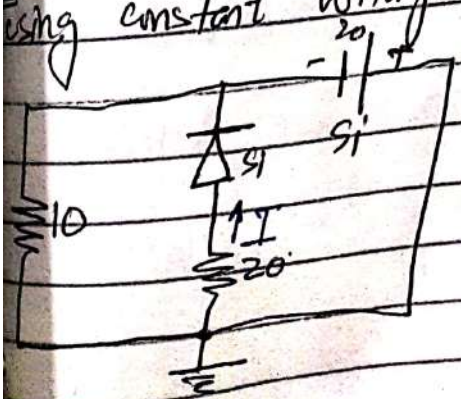
If the direction of diode is reversed;



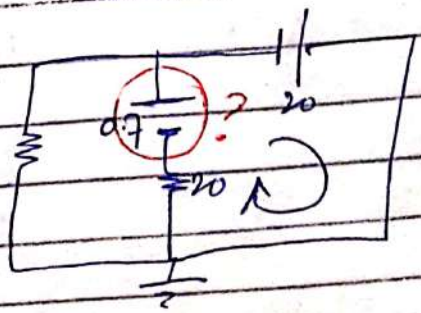
Directions are not matching so diode is off and its equivalent model is an open circuit.

$I_D = 0$ and $V_R = 0$

Determine the current I in the shown configuration using constant voltage drop model.



Diode is ON → V_b

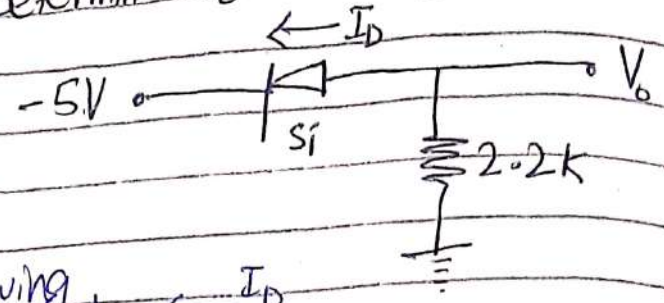


KVL to the loop

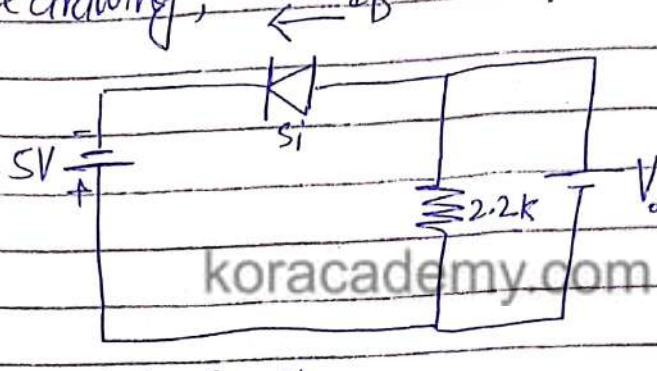
20V $-20I - 0.7V = 0$

$\Rightarrow I = 965mA$

Q. Determine V_o and I_D.

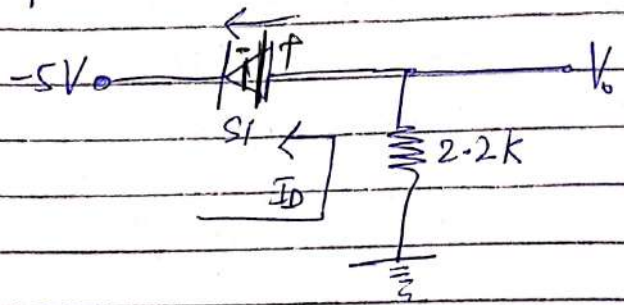


Redrawing,



Diode is ON

Equivalent Circuit;



$-5V + 0.7V = V_o$

$\Rightarrow \boxed{V_o = -4.3V}$

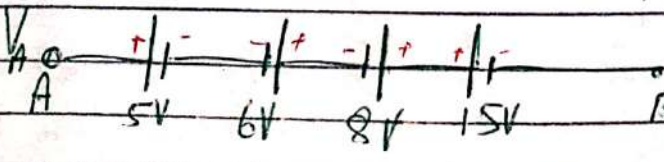
Similarly

$0V - 2.2I_D = V_o$

$-2.2I_D = -4.3V \Rightarrow \boxed{I_D = 1.95m}$

How to deal with potential at points?

eg



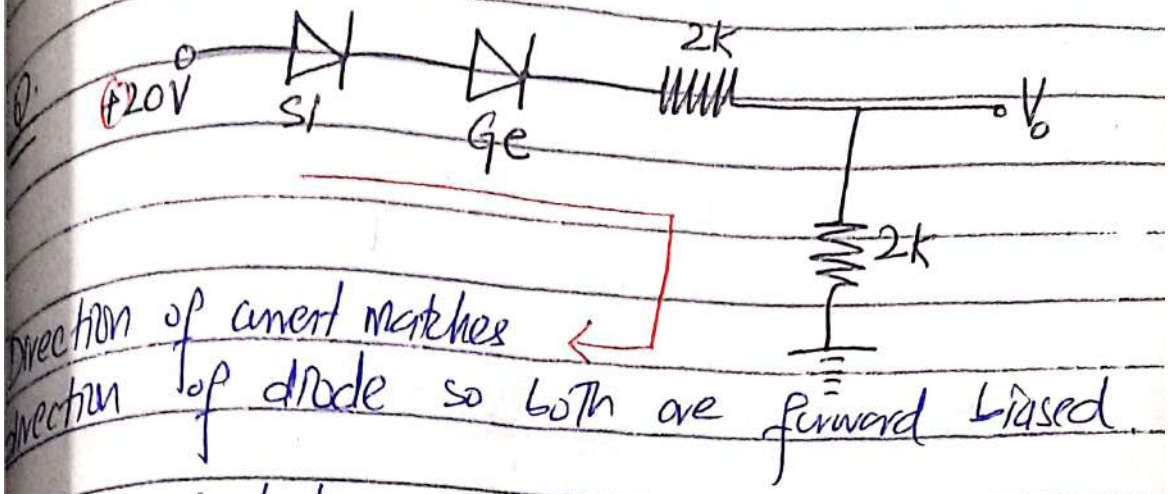
$V_A - V_B = ?$

Starting from V_A;

$$V_A - 5V + 6V + 8V - 15V = V_B$$
$$V_A - V_B = 6V$$

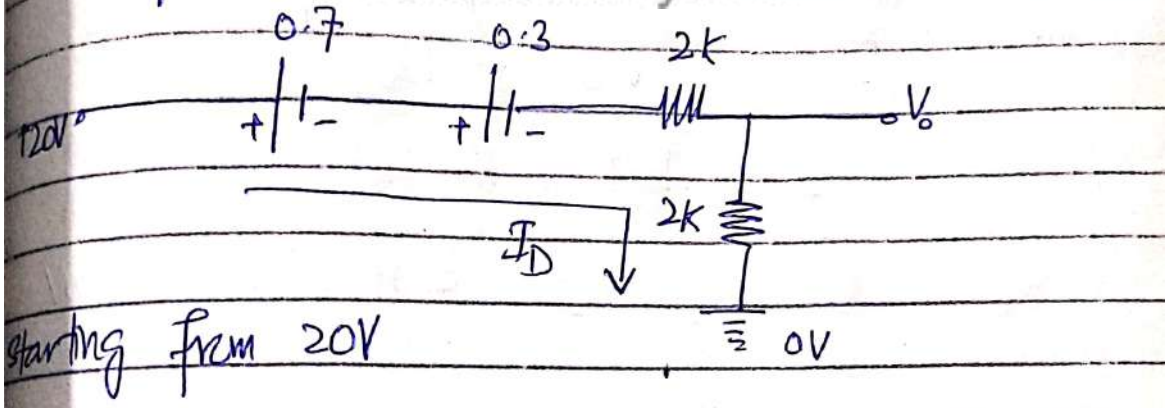
let $V_b = 4V \Rightarrow V_A = 10V$.

Q.



Direction of current matches direction of diode so both are forward biased

The equivalent model is as;



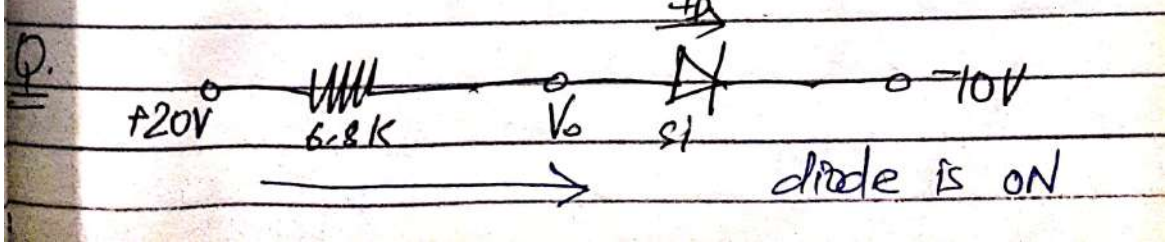
Starting from 20V

$$20V - 0.7V - 0.3V - 2I_D - 2I_D = 0$$
$$\Rightarrow I_D = 4.75mA$$

Similarly $V_o - 2I_D = 0$

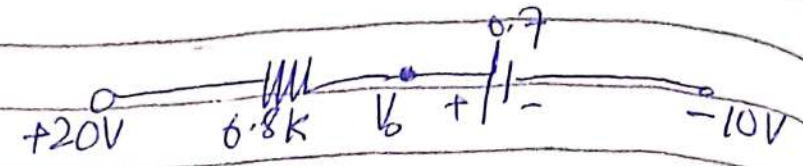
$$\Rightarrow V_o = 9.5V$$

Q.



diode is ON

equivalent circuit;

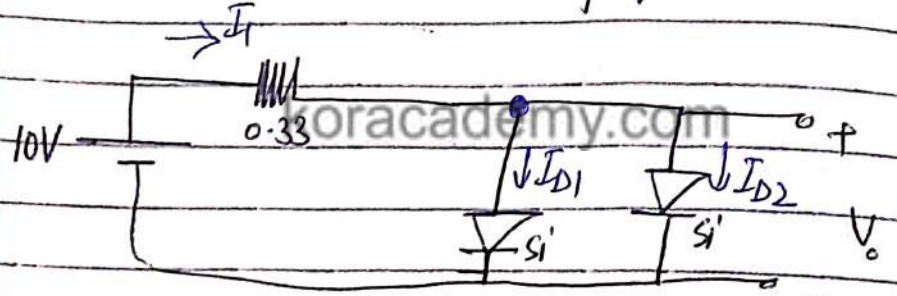


$$20V - 6.8 I_D - 0.7V = -10V$$
$$\Rightarrow I_D = 4.30\,mA$$

For V_o

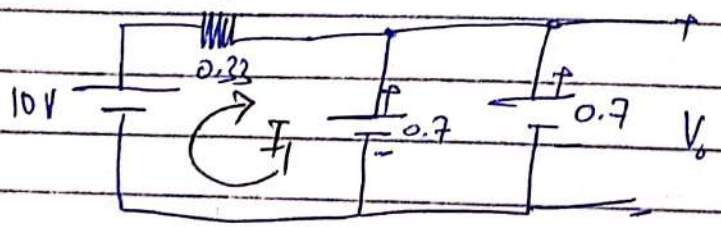
$$20V - 6.8 I_D = V_o$$
$$\Rightarrow V_o = -9.3\,V$$

Parallel Diode Configurations.



$V_o, I_1, I_{D1}, I_{D2} = ?$ Both diodes are ON

The equivalent model



$V_o = 0.7\,V$

For I_1,

$10V - 0.33 I_1 - 0.$

$\Rightarrow I_1 = 28.8m$

KCL at the node;

$$I_1 = I_{D1} + I_{D2}$$

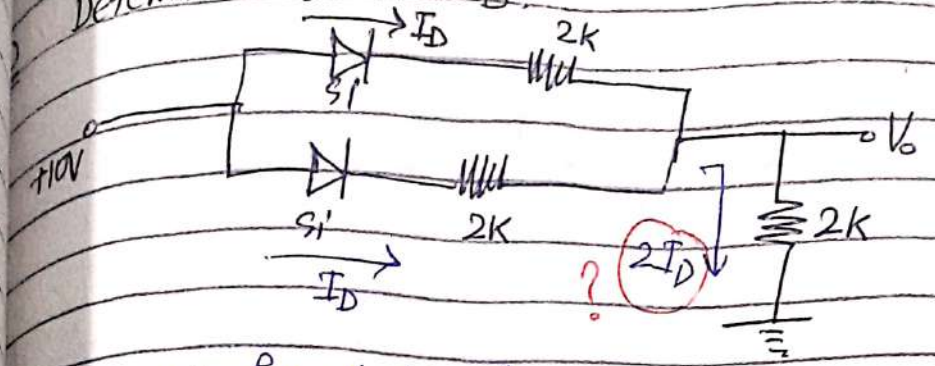
As $I_{D1} = I_{D2}$ let I_D

$$I_1 = 2 I_D$$

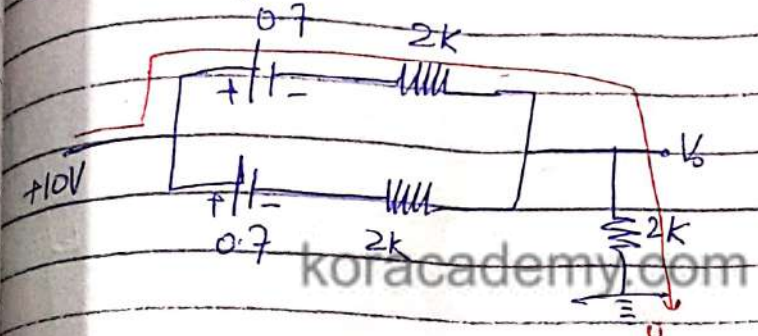
$$\Rightarrow I_D = \frac{I_1}{2} = \frac{28.18}{2} = 14.09\,mA.$$

Parallel and Series Parallel Configurations.

Determine V_o and I_D.



Diodes are forward biased → ON



$+10V - 0.7V - 0.7V - 2I_D - 4I_D = 0$

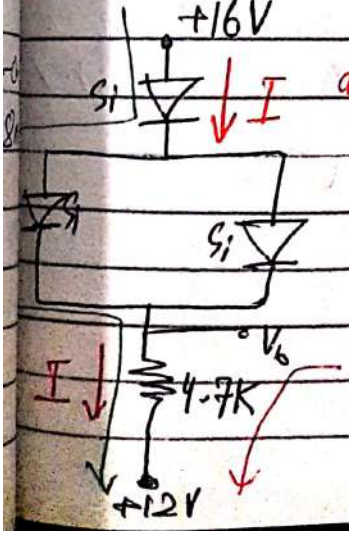
$I_D = 1.55mA$

Also

$V_o - 4I_D = 0$

$\Rightarrow V_o = 6.2V.$

Q. Determine V_o and I



as $16 > 12$

$\rightarrow 16V - 0.7V - 0.7V - 4.7I = 12V$

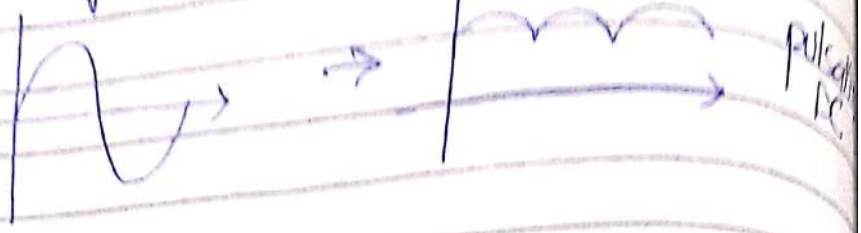
$\Rightarrow I = 0.55mA$

$\rightarrow V_o - 4.7I = 12V$

$\Rightarrow V_o = 14.6V$

Introduction to Rectifier Circuits

Rectification → correction of error
eg when we rectify (correct) AC voltage
you get DC voltage.

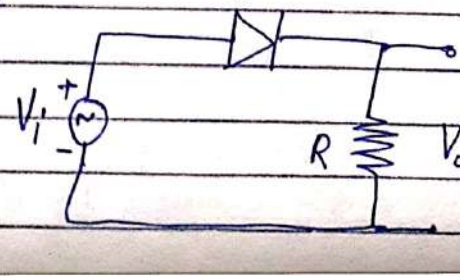


After filteration we have pure dc

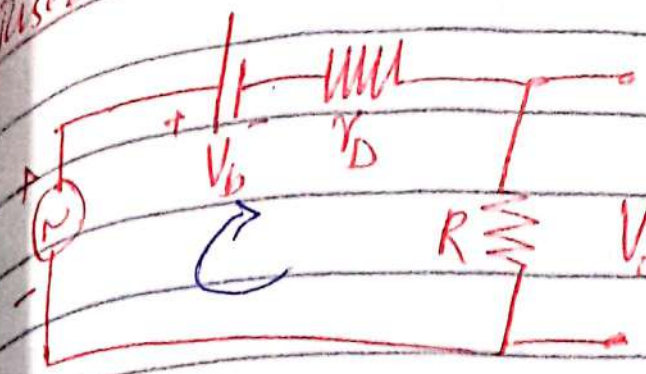
Three types of rectifier circuits.
(i) Half wave " "
(ii) Full wave " " → Center tap
→ Bridge type

Half Wave Rectifier

In HWR, only one half of the ac voltage is rectified, for the other half we get zero voltage.



For +ve half cycle → diode is forward biased.



$$V_i - V_b - I r_D - IR = 0$$

$$I = \frac{V_i - V_b}{r_D + R}$$

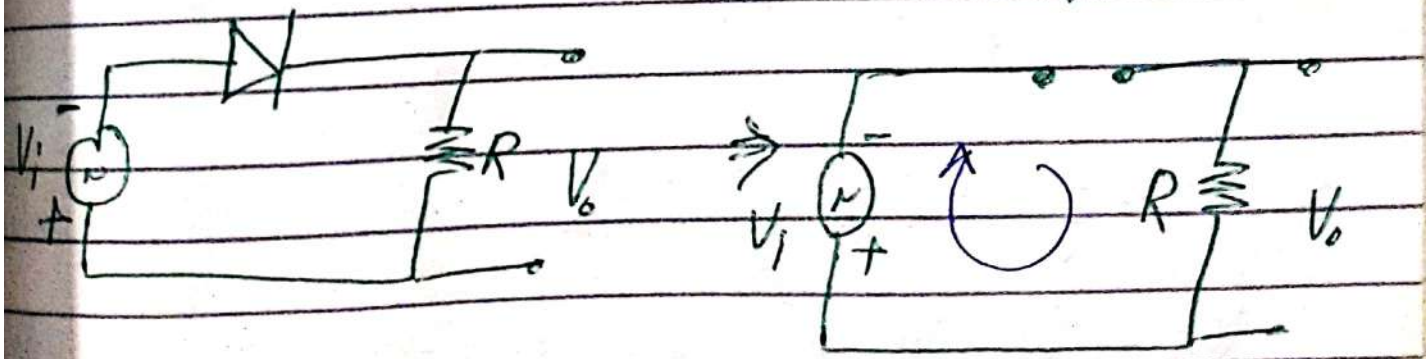
$$V_o = IR$$

$$V_o = \left(\frac{V_i - V_b}{r_D + R}\right) \times R$$

$$\Rightarrow V_o = \left(\frac{R}{r_D + R}\right) V_i - \left(\frac{R}{r_D + R}\right) V_b$$

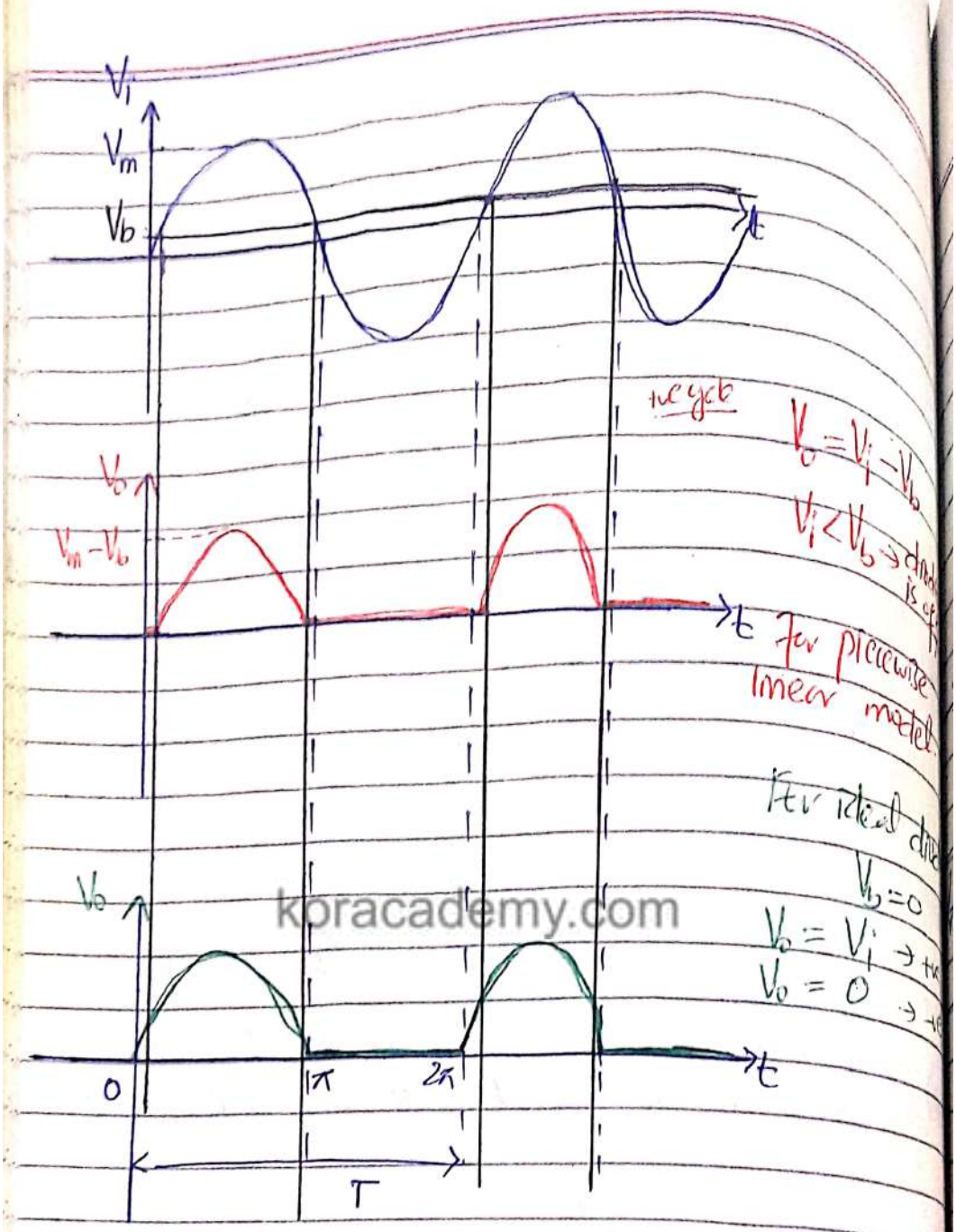
As $r_D << R$ $\Rightarrow$ $\boxed{V_o = V_i - V_b}$

For negative half cycle, the diode is reverse biased, and act as open circuit.



As $I = 0$ $\Rightarrow$ $V_o = IR = (0)R$

$\Rightarrow$ $\boxed{V_o = 0}$



+ve cycle

$V_o = V_i - V_b$

$V_i < V_b \rightarrow$ diode is off

for piecewise linear model

for ideal diode

$V_b = 0$

$V_o = V_i \rightarrow$ +ve

$V_o = 0 \rightarrow$ -ve

Average output voltage

$V_o = V_m \sin\omega t \qquad 0 \le \omega t < \pi$

$V_o = 0 \qquad \pi \le \omega t \le 2\pi$

$$\Rightarrow V_{av} = \frac{1}{2\pi} \int_0^{2\pi} V_o \, d\omega t$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} V_m \sin\omega t \, d\omega t + \int_{\pi}^{2\pi} 0 \, d\omega t \right]$$

$$= \frac{1}{2\pi} \int V_m \sin\omega t \, d\omega t$$

$$= \frac{V_m}{2\pi}\left(-\cos\omega t\right|_0^{\pi}$$

$$= \frac{V_m}{2\pi}\left(-\cos\pi - (-\cos 0)\right) = \frac{V_m}{2\pi} \times 2.$$

$$\Rightarrow \boxed{V_{avg} = \frac{V_m}{\pi} = 0.318\, V_m}$$

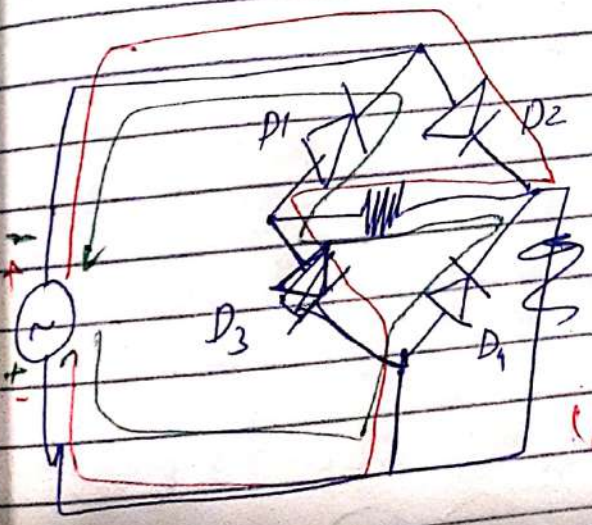
Average load current

$$I_{avg} = \frac{V_{avg}}{R} = \frac{V_m}{\pi} \div R = \frac{V_m}{\pi R}$$

$$\boxed{I_{rms} = \frac{V_m}{2}} \Rightarrow \boxed{I_{avg} = \frac{I_m}{\pi}} \qquad \boxed{I_{rms} = \frac{I_m}{2}}$$

Full Wave Bridge Rectifier-

→ Ripple factor in H.W.R is 121%.
→ Efficiency of H.W.R is 40.56%.



the HC
D_2 and D_3
forward biased
& closed ckt.

KVL (ideal) $+V_i - V_o = 0$

$\boxed{V_o = V_i}$

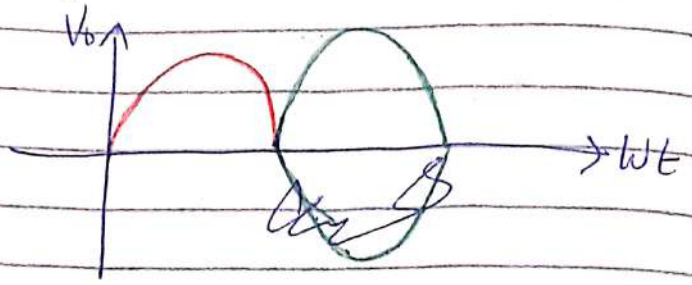
for constant voltage drop model $\boxed{V_o = V_i - 2V_b}$

For piecewise linear model

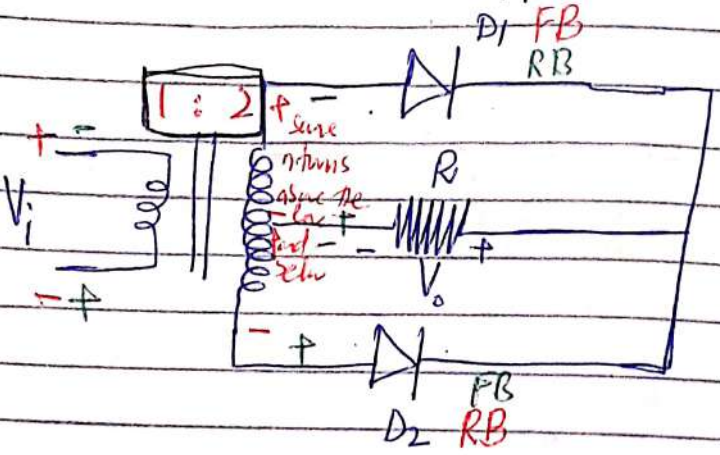
$$V_o = V_i - 2V_\gamma - 2IR_d$$

For negative half cycle D_1 and D_4 will be forward biased.

$$\therefore V_o - V_i = 0 \Rightarrow \boxed{V_o = V_i}$$

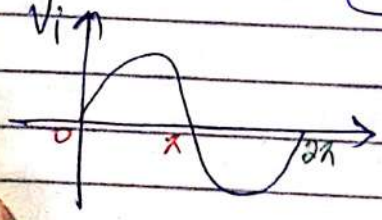


Full Wave Center Tapped Rectifier



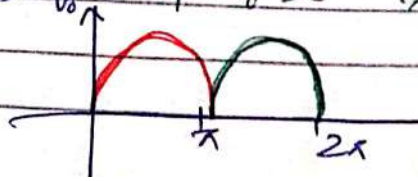
$$\frac{N_p}{N_s} = \frac{V_p}{V_s} \Rightarrow \frac{1}{2} = \frac{V_i}{V_s}$$

$$\Rightarrow \boxed{V_s = 2V_i}$$



$+V_o - V_i = 0 \Rightarrow V_o = V_i$

$+V_i - V_o = 0 \Rightarrow V_o = V_i$



Parameters

Average (dc) load voltage

$V_o = V_m \sin\omega t \quad 0 \le \omega t \le \pi$

$$V_{av} = V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_m \sin\omega t \, d\omega t$$

$$\boxed{V_{av} = \frac{2V_m}{\pi}}$$

Average load current

$$I_{avg} = \frac{V_{av}}{R} = \frac{2V_m}{\pi R}$$

$$\Rightarrow \boxed{I_{av} = \frac{2I_m}{\pi}}$$

Rms load current

$$\boxed{I_{rms} = \frac{I_m}{\sqrt{2}}}$$

Rms load voltage

$$V_{rms} = I_{rms} R = \frac{I_m}{\sqrt{2}} \times R$$

$$\Rightarrow \boxed{V_{rms} = \frac{I_m R}{\sqrt{2}}} \qquad \boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

Form factor of full wave rectifier

$$F.F = \frac{V_{rms}}{V_{av}} \quad \text{or} \quad \frac{I_{rms}}{I_{av}}$$

As $V_{rms} = V_m/\sqrt{2}$ and $V_{av} = 2V_m/\pi$

$$\Rightarrow F.F = \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\sqrt{2}}{2/\pi}$$

$$\boxed{F.F = 1.1}$$

Ripple Factor

%age of AC component in the rectified output.

ac → dc

↳ ideally ac = 0 ⇒ $\gamma = 0$

$$\gamma = \sqrt{(F.F)^2 - 1}$$

$$\gamma\% = \sqrt{(F.F)^2 - 1} \times 100\%$$

As $F.F = 1$ ⇒ $\boxed{\gamma\% = 48.1\%}$

For half wave rectifier

$$\boxed{\gamma\% = 121\%}$$

Efficiency = $\frac{\text{output dc power}}{\text{input ac power}} \times 100\%$

As $P = I^2R \Rightarrow \eta = \frac{I_{dc}^2 R}{I_{rms}^2 R}$

As $I_{dc} = \frac{2I_m}{\pi}$ $\quad I_{rms} = \frac{I_m}{\sqrt{2}}$

$\eta = \frac{4I_m^2/\pi^2}{I_m^2/2} \times 100\% = \frac{8}{\pi^2} \times 100\%$

$\Rightarrow \boxed{\eta = 81.13\%}$

Efficiency of half wave rectifier

$\boxed{\eta = 40.58\%}$

Peak Inverse voltage

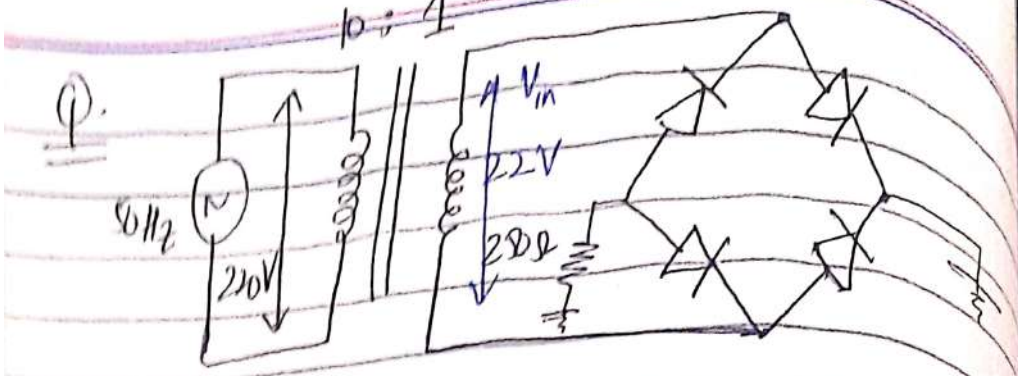
For full wave bridge rectifier circuit;

$\boxed{PIV \geq V_m}$

For centre taped circuit;

$\boxed{PIV \geq 2V_m}$

Q.



Calculate; Assuming the diodes are ideal;

(a) dc output voltage. (V_{dc} or V_{avg})

$f_{in} = 50\,Hz$ $\quad \frac{N_p}{N_s} = \frac{10}{1}$

$\therefore \frac{N_p}{N_s} = \frac{V_p}{V_s} = \frac{10}{1} = \frac{220}{V_s}$

$\Rightarrow V_s = \frac{220}{10} \Rightarrow \boxed{V_s = 22V}$

$\therefore V_{av} = V_{dc} = \frac{2V_m}{\pi}$ → peak or maxim

$\therefore V_{rms} = \frac{V_m}{\sqrt{2}} = 22 \Rightarrow V_m = 22 \times \sqrt{2}$

$\Rightarrow \boxed{V_m = 31.11\,V}$

$V_{dc} = \frac{2(31.11)}{3.14} \Rightarrow \boxed{V_{dc} = 19.81}$

(b) Rectification efficiency ($\eta\%$)

$\eta = \frac{P_{out}}{P_{in}} = \frac{I_{dc}^2 R}{I_{rms}^2 R} = \frac{V_{dc}^2/R}{V_{rms}^2/R}$

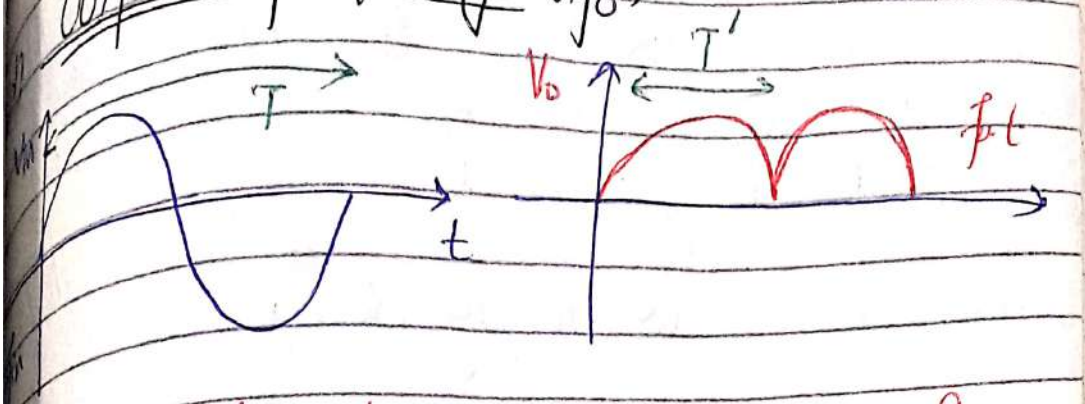
$\eta\% = \frac{V_{dc}^2}{V_{rms}^2} \times 100\% = \frac{(19.81)^2}{(22)^2}$

$\Rightarrow \boxed{\eta = 81.08\%}$

Peak inverse voltage (PIV)

$PIV \geq V_m \Rightarrow PIV \geq 31.1$ volts.

Output frequency (f_o)



Time period → time taken by a waveform repeat itself.

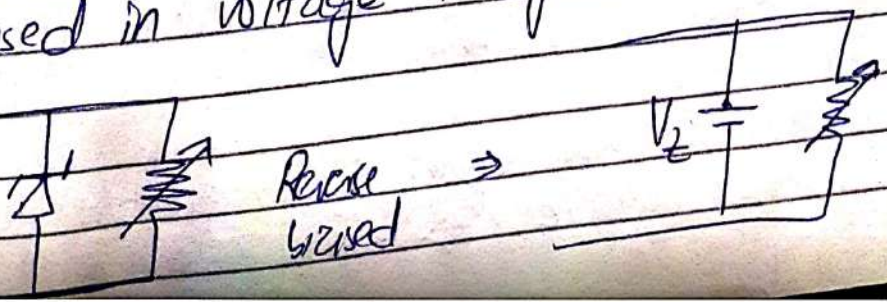
$$T' = \frac{1}{2}T \Rightarrow T = 2T'$$

$$f = \frac{1}{T} \Rightarrow T = \frac{1}{f} \quad \frac{1}{f_m} = \frac{1}{2} \frac{1}{f_o}$$

$$\Rightarrow f_o = 2 f_m \Rightarrow \boxed{f_o = 100\ Hz}$$

Introduction to Zener Diode

Zener diode is a special diode → widely used in voltage regulation.



Two types of breakdown.

(i) Avalanche breakdown.

We apply a high reverse bias potential across the diode → The electrons gain high kinetic energy and break the covalent bond and they also free more electrons due to collisions and we have a chain reaction and because of this large current is produced.

Occurs in lightly doped diodes (normal diodes)

Zener diodes are highly doped diodes.

(ii) Zener Breakdown.

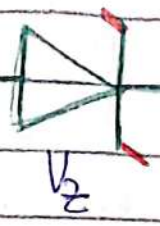
Here we can achieve the breakdown much earlier because we increase the doping level on both (P and N) sides.

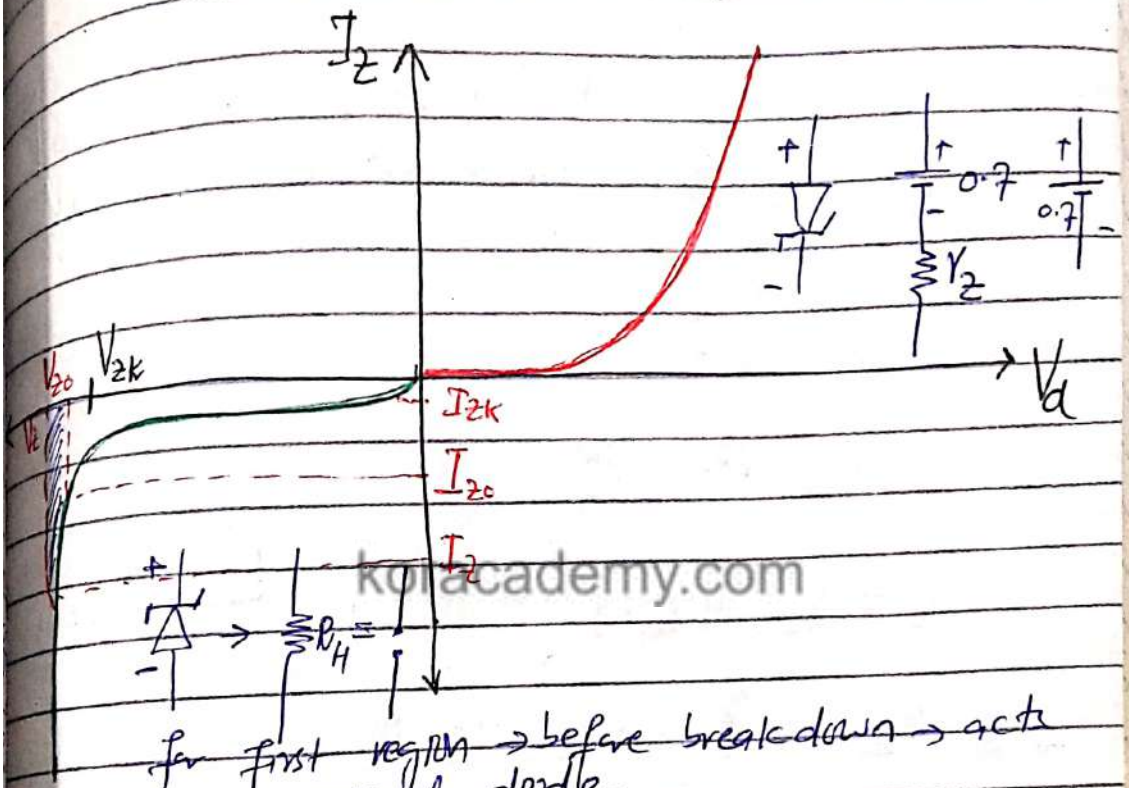
Breakdown is initiated by direct rupture of covalent bonds. → happens due to strong electric field at the junction developed by high reverse bias potential.

- High power dissipation capability. → they can easily work in breakdown region.
- Properties will not degrade → As a normal diode does not work when reverse biased but zener diode will.
- In forward bias region, zener diode acts as normal diode. → similar characteristics

Zener diode acts as voltage regulator when we make it in reverse bias region.

Symbol



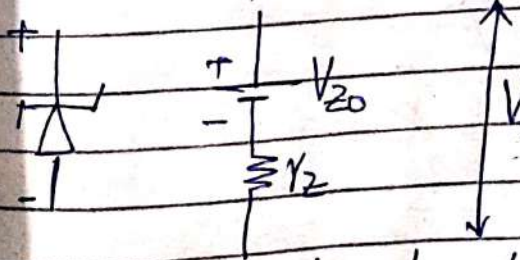


for first region → before breakdown → acts as a normal diode.

V_{zk} → voltage after which breakdown occurs.

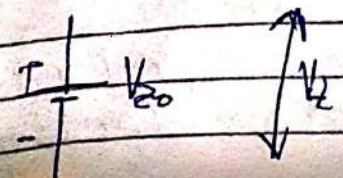
I_{zk} → knee current

$$V_z = V_{z0} + r_z \times I_z$$

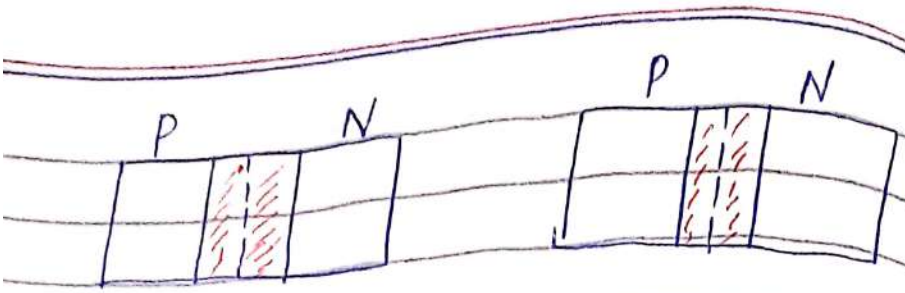


$$r_z = \frac{1}{\text{slope}}$$

If r_z is considered to be very small.

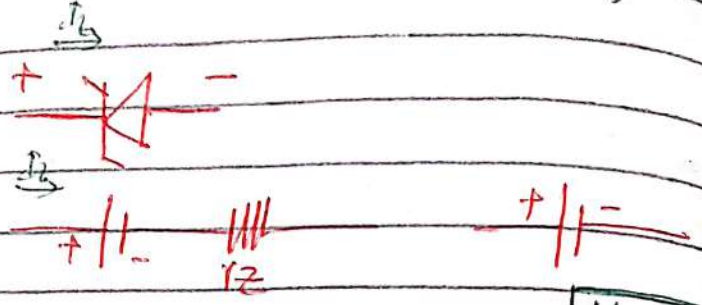


$$V_z = V_{z0}$$



Normal diode zener diode → depletion layer is narrower than normal diode

eg for normal diodes breakdown voltage > 6V
for zener diodes breakdown voltage < 6V



$V_z = V_{z0} + I_z r_z$

$V_z = V_{z0}$

Temperature effects on zener voltage

The breakdown voltage of a zener diode is very sensitive to the temperature of operation.

If we change the temperature, the breakdown voltage will also change

$$T_c = \frac{\Delta V_z / V_z}{T_1 - T_0} \times 100\% \ /^\circ C$$

→ temperature coefficient

ΔV_z → change in zener voltage.

V_z → zener voltage at room temperature (25°)

T_1 → new temp T_0 → initial (room) temperature

Calculate the change in zener voltage if zener voltage is 10V at 25°C and new temp is 100°C. Temp coefficient (T_c) is 0.072 %/°C

$\Delta V_z = ?$ $V_z = 10V$ $T_1 = 100°C$ $T_0 = 25°C$

$T_c = 0.072$ %/°C

$$\Delta V_z = \frac{T_c V_z}{100\%} (T_1 - T_0)$$

$$= \frac{(0.072)(10)}{100\%} (100° - 25°C)$$

$$\boxed{\Delta V_z = 0.54\ V}$$

Zener Diode As Voltage Regulator:

Voltage regulator?

It is a combination of elements designed to ensure that the output voltage of a supply remains constant.

Two regions in reverse bias condition;

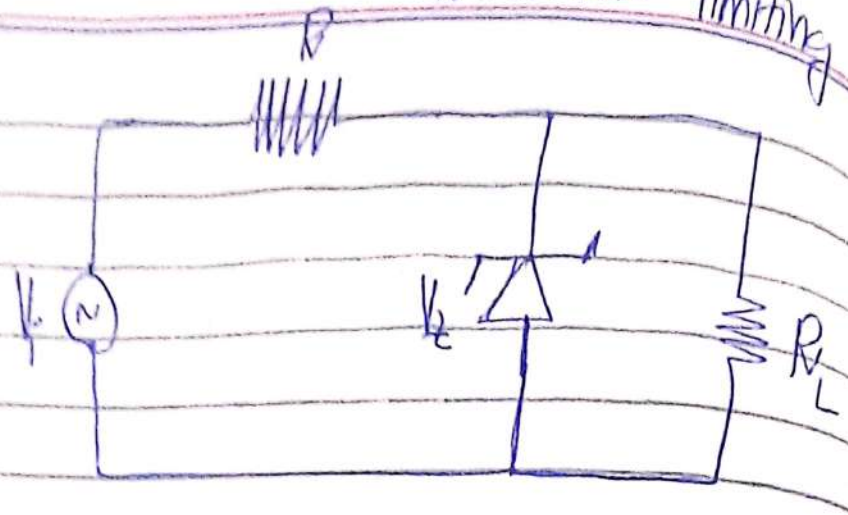
i) When there is no breakdown → zener diode is off.

ii) After breakdown → diode is ON.

So important to provide reverse bias potential greater than the zener potential (V_z).

Understanding a basic regulator circuit;

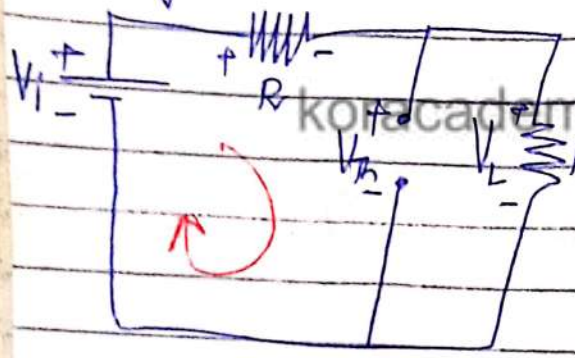
R_s → current limiting resistor



Four cases depending on V_i and R_L.

① V_i and R_L both are fixed.

Using thevenin's theorem;



$V_i - IR_s - IR_L = 0$

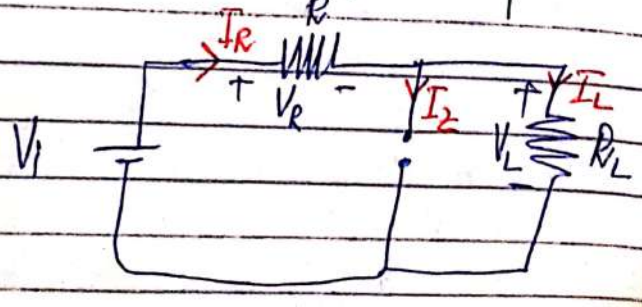
$I = \frac{V_i}{R_s + R_L}$

$V_{Th} = V_L = IR_L \Rightarrow V_{Th} = \frac{V_i R_L}{R_s + R_L}$

If $V_{Th} \geq V_z$ → diode is ON → breakdown

If $V_{Th} < V_z$ → diode is OFF → no breakdown

When diode is off, so open circuit in place of



$I_Z = 0$

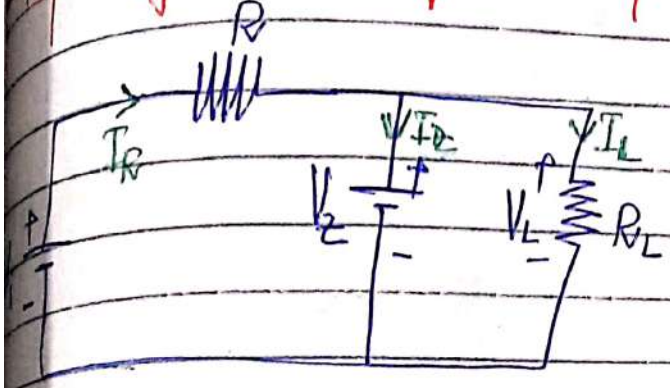
$P_Z = 0$

KCL $I_R = I_L$

$$I_R = \frac{V_i}{R + R_L} = I_L$$

$V_L = I_R R$ $\quad V_L = I_R R_L$

Replacing diode by its equivalent circuit.



KCL

$I_R = I_L + I_Z$

$$I_Z = I_R - I_L$$

$$I_R = \frac{(V_i - V_Z)}{R} \qquad I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L}$$

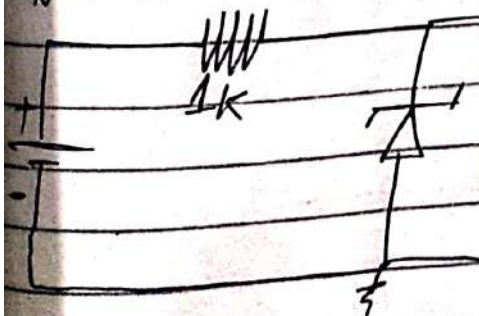
$(V_Z = V_L)$

$$I_Z = \frac{(V_i - V_Z)}{R} - \frac{V_Z}{R_L}$$

Also $P_Z = I_Z V_Z$

$P_Z < P_{Zm}$

2. For the zener diode network, determine V_L, V_R, I_Z and P_Z. If $V_Z = 10V$ $P_{Zm} = 30mW$

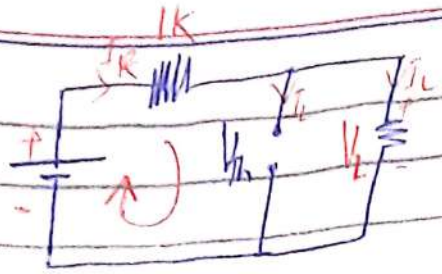


$V_i = 16V$ $R = 1k\Omega$

$R_L = 1.2k\Omega$

$V_Z = 10V$

First find state of diode by using thevenins theorem → open ckt the diode.



$16 - I(1K) - I(1.2K) = 0$

$I = \frac{16}{1+1.2} \Rightarrow \boxed{I = 7.27\,mA}$

$V_{Th} = V_L = I \times 1.2k = (7.27m)(1.2k)$

$\Rightarrow \boxed{V_{Th} = 8.72V}$

$V_{Th} < V_z \rightarrow$ diode is off

Case ① $\Rightarrow I_z = 0$ and hence $P_z = 0$.

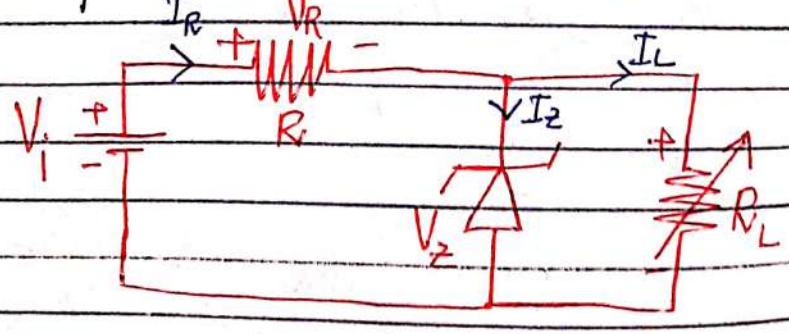
KCL $I_R = I_L$ $\quad V_R = I_R \times 1k\Omega$

$I_R = \frac{16}{1+1.2k} \Rightarrow \boxed{I_R = 7.27\,mA}$

$V_R = 7.27mA \times 1.2k \Rightarrow \boxed{V_R = 7.27V}$

$V_L = I_L \times 1.2k = (7.27)(1.2) \Rightarrow \boxed{V_L = 8.64V}$

② V_i is fixed, R_L is variable



When load resistance (R_L) is too small voltage across zener diode will be smaller than V_z and so the diode will be OFF.

$R_L = 0$ ⇒ $V_{Th} = 0$ ⇒ Zener diode will be shorted

So we need to find minimum load resistance which will turn the diode ON and then we will find the maximum load resistance.

Condition for minimum load resistance (R_L)

minimum voltage to turn zener diode ON is V_Z.

Applying Thevenin's theorem; $V_{Th} = \frac{V_i R_L}{R + R_L} = V_Z$

$V_Z = V_L$

$V_Z = \frac{V_i R_L}{R + R_L} \Rightarrow V_Z(R + R_L) = V_i R_L$

$V_Z R + V_Z R_L = V_i R_L \Rightarrow V_i R_L - V_Z R_L = V_Z R$

$$R_{L_{min}} = \frac{V_Z R}{V_i - V_Z}$$

⇒ current will be maximum.

$$I_{L_{max}} = \frac{V_L}{R_{L_{min}}} = \frac{V_Z}{R_{L_{min}}}$$

KCL to the only node

⇒ $I_R = I_{Z_{min}} + I_{L_{max}}$

$I_{Z_{min}} = I_R - I_{L_{max}}$

$= V_i - V_Z - I_{L_{max}}$.

Condition For maximum load resistance

$$R_{L_{max}} \Rightarrow I_{L_{min}} \Rightarrow I_{Z_{max}}$$

We know that

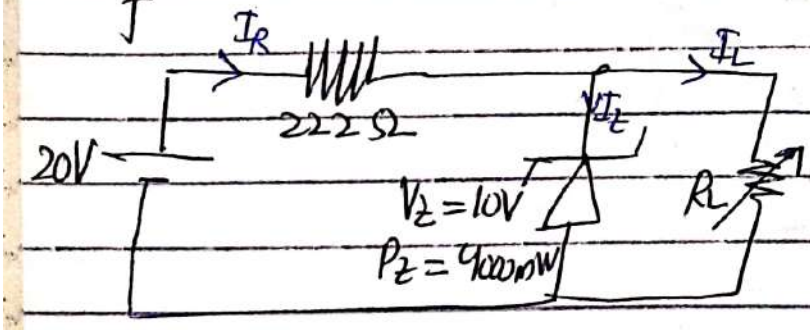
$$P_{Z_{max}} = I_{Z_{max}} V_Z$$

$$\Rightarrow \frac{P_{Z_m}}{V_Z} = I_{Z_{max}}$$

$$\boxed{I_{L_{min}} = I_R - I_{Z_{max}}} = \left(\frac{V_i - V_Z}{R}\right) - \frac{P_{Z_m}}{V_Z}$$

$$\boxed{R_{L_{max}} = \frac{V_L}{I_{L_{min}}} = \frac{V_Z}{I_{L_{min}}}}$$

Q. Determine the minimum and maximum values of load resistance R_L.



$R = 222\ \Omega$
$V_i = 20\ V$
$V_Z = 10\ V$
$P_{Z_M} = 400\ mW$

$$R_{L_{min}} = \frac{V_Z R}{V_i - V_Z} = \frac{(10)(222)}{20 - 10}$$

$$\Rightarrow \boxed{R_{L_{min}} = 222\ \Omega}$$

$$I_{L_{max}} = \frac{V_Z}{R_{L_{min}}} = \frac{10}{222} \Rightarrow \boxed{I_{L_{max}} = 45mA}$$

$R_{L\,max}$?

$P_{zm} = I_{zm} V_z \Rightarrow 400mW = I_{zM} \times 10$

$\Rightarrow \boxed{I_{zM} = 40mA}$

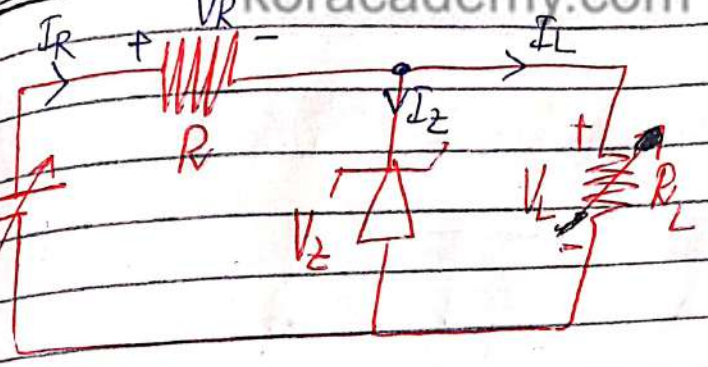
$I_{L_{min}} = I_R - I_{z_{max}} = 45mA - 40mA$

$I_R = V_i - V_z / R$

$\boxed{I_{L\,min} = 5mA}$

$R_{L\,max} = \frac{V_z}{I_{L\,min}} = \frac{10}{5mA} \Rightarrow \boxed{R_{L_{max}} = 2k\Omega}$

3) Variable V_i and Fixed R_L



Condition for minimum input voltage.
The least value of V_i required to turn the diode ON.

Thevenins theorem $V_{th} \Rightarrow V_z \rightarrow ON$
↳ minimum

$V_{th} = \frac{V_i R_L}{R + R_L} = V_z$

$\Rightarrow \boxed{V_{i_{min}} = \frac{V_z (R + R_L)}{R_L}}$

Condition For Maximum Voltage V_i

The maximum input voltage is limited by the value of maximum zener current.

KCL $\quad I_{R_{max}} = I_{Z_{max}} + I_L$

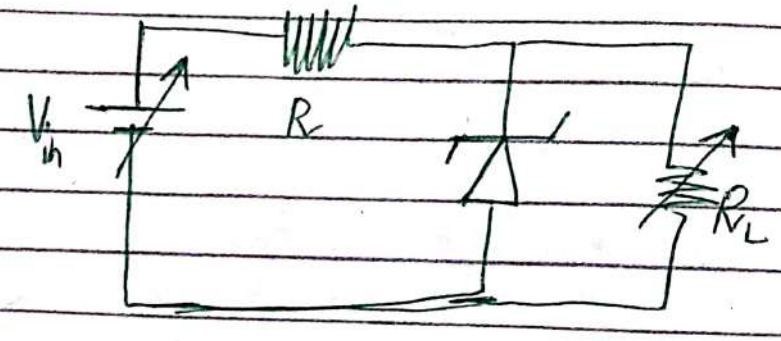
$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L}$ $\quad V_Z \rightarrow$ mentioned in data, $I_L, R_L \rightarrow$ fixed

KVL $\quad V_{i_{max}} - V_{R_{max}} - V_Z = 0$

$V_{i_{max}} = V_{R_{max}} + V_Z$

$V_{R_{max}} = I_{R_{max}} R_s \Rightarrow$ $\boxed{V_{i_{max}} = I_{R_{max}} R_s + V_Z}$

(4) Both V_i and R_L are Variable



Under such condition, we have to calculate the dynamic range of current limiting resistance R_s (series resistance)

$$R_{min} = \frac{V_{i_{max}} - V_Z}{I_{R_{max}}}$$

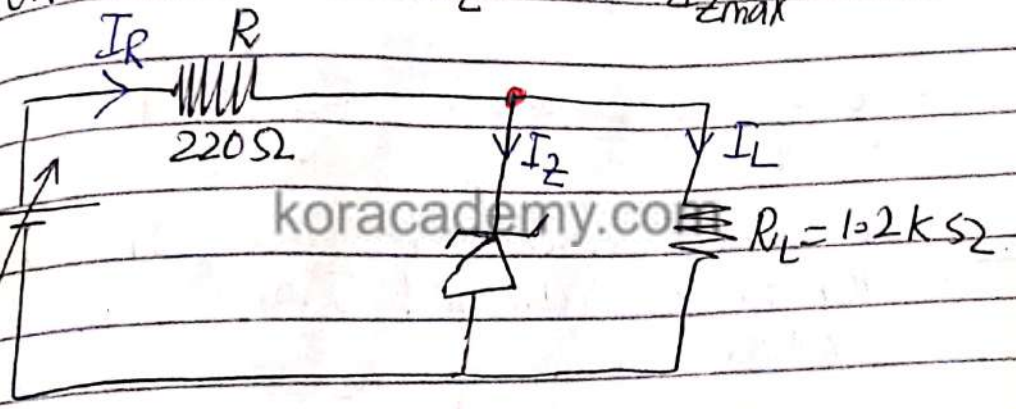
$$R_{max} = \frac{V_{imin} - V_z}{I_{R\,min}}$$

Variable problems in zener diodes:

$$I_R \geq I_L + I_z$$

$$\frac{V_i - V_z}{R} \geq I_L + I_z$$

Determine the range of input voltage (V_i) that will maintain zener diode ON state. $V_z = 20V$ $I_{zmax} = 60mA$



As $V_{imin} = \frac{V_z(R + R_L)}{R_L} = \frac{20(220 + 1.2k)}{1200}$

$\Rightarrow V_{imin} = 23.67\ V$

$V_{imax} = V_{Rmax} + V_z$

$= I_{Rmax} R + V_z \rightarrow (1)$

KCL $I_R = I_z + I_L$

$I_{zmax} \geq I_{Rmax}$ B/C I_L is fixed.

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20}{1200}$$

$$\Rightarrow I_L = 16.67\,mA$$

$$\Rightarrow I_{R_{max}} = 60mA + 16.67mA$$

$$\Rightarrow I_{R_{max}} = 76.67\,mA$$

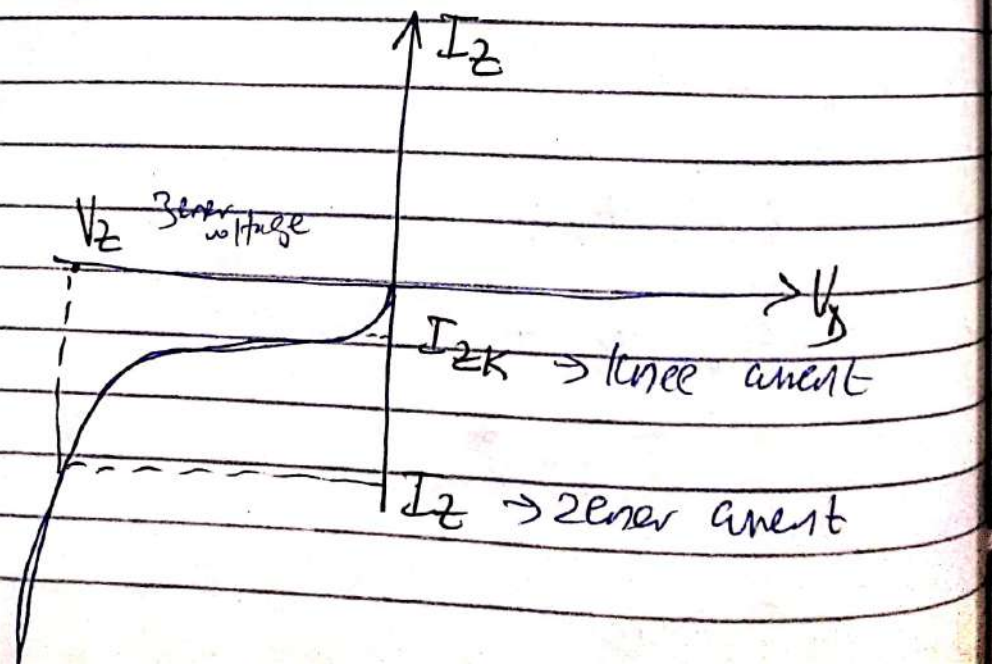
$$\textcircled{1} \Rightarrow V_{i_{max}} = (76.67\,m)(220) + 20$$

$$\Rightarrow V_{i_{max}} = 36.867\,V.$$

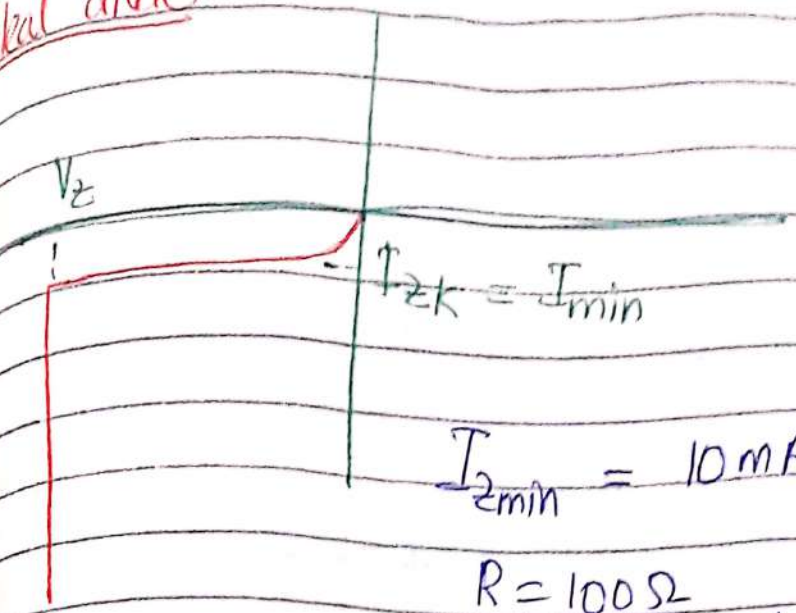
Range of $V_i = 23.67 - 36.86$ Volts.

Q. The knee current of ideal zener diode is 10mA. To maintain 5 volts across R_L, the minimum value of R_L and minimum power rating of the diode are;

For normal zener diode



Ideal diode

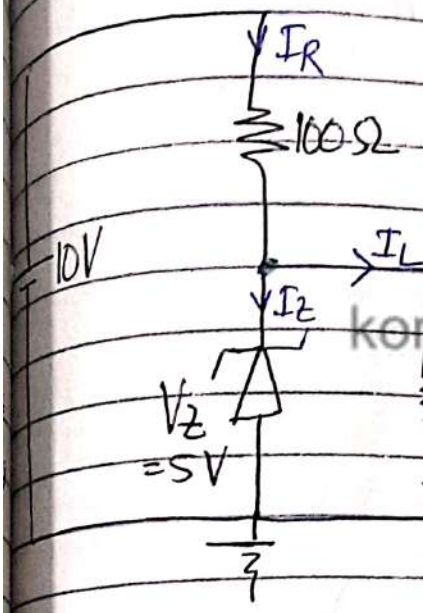


$I_{zmin} = 10mA$

$R = 100\Omega$

$V_z = 5V \quad V_i = 10V$

$R_{L_{min}} = ?$



$R_{L_{min}} \Rightarrow I_{L_{max}}$

$\Downarrow$

$I_{z\,min}$

KCL

$I_R = I_{z_{min}} + I_{L_{max}}$

$\downarrow$

$I_R = \frac{V_i - V_z}{R} \Rightarrow \frac{10-5}{100} = 10mA + I_{L_{max}}$

$\Rightarrow I_{L_{max}} = 40mA$

$R_{L_{min}} = \frac{V_L}{I_{L_{max}}} = \frac{V_z}{I_{L_{max}}} = \frac{5V}{40m}$

$\Rightarrow \boxed{R_{L_{min}} = 125\Omega}$

Power rating

$Power = I_{z_{max}} \times V_z$

$I_{C(max)} = 50mA$

B/C $50mA = I_E + I_C$

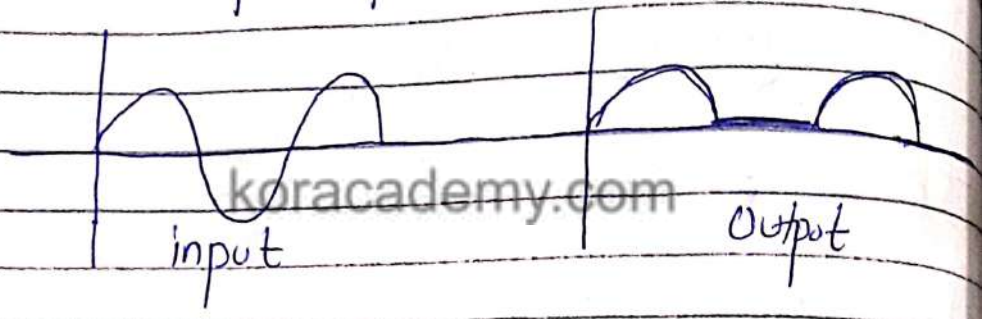
V_0

Power = 50 mA x 5V

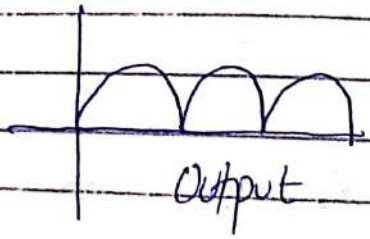
= 250 mW

Introduction To Clippers.

In case of half wave rectifier;



Full wave rectifier.



We use diodes along with resistors and capacitors to shape waveforms. → circuits are called wave shaping circuits.

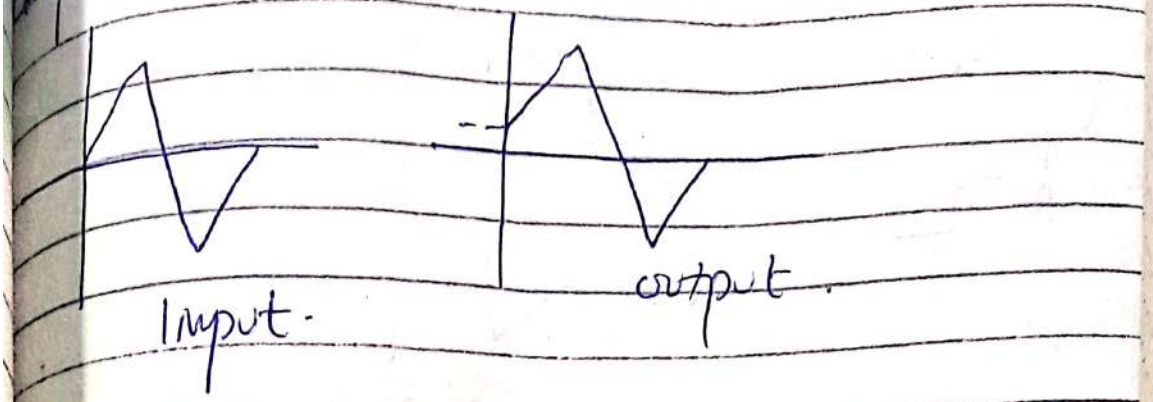
Clippers and clampers are wave shaping circuits.

If we want to clip portion of the waveform we use clippers and if we want to shift or clamp the dc. with

level we use clampers.

Half wave rectifier is the simplest example of clipper circuit in which we clipp off the negative half cycle.

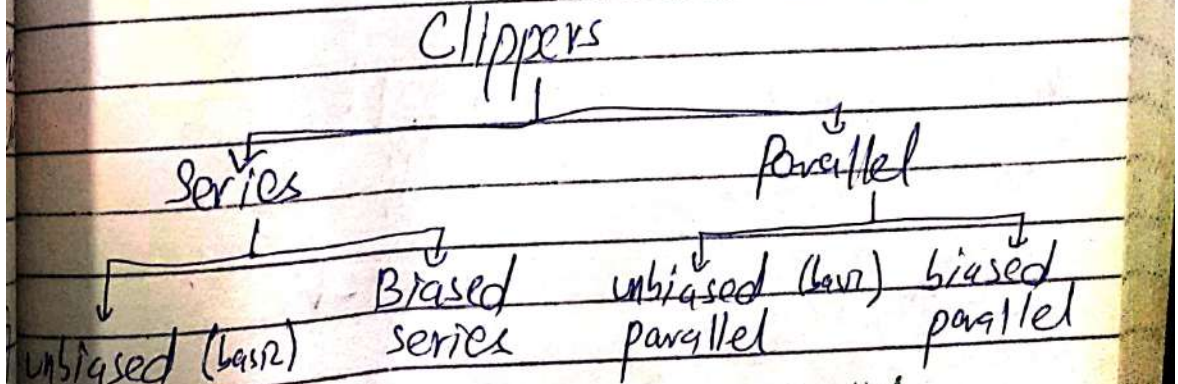
Clampers;



Clippers

Clippers are networks that use diodes to clip a portion of input signal without disturbing the remaining part of the waveform.

Eg in H.W.R the negative cycle is clipped whereas the positive is not disturbed.



Series → diode is connected in series with load resistance.

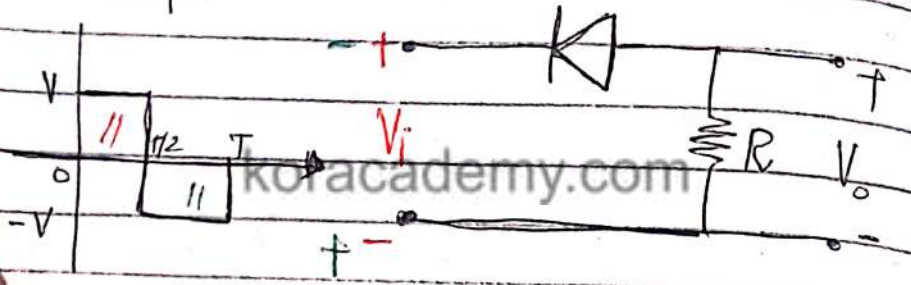
Parallel

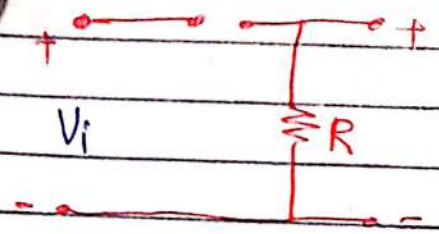
In case of biased clippers, there is additional dc source present in the clipper circuit.

All these few are further classified into
i. Positive clippers. → +ve portion of wave is clipped
ii. Negative clippers. → -ve portion of waveform is clipped

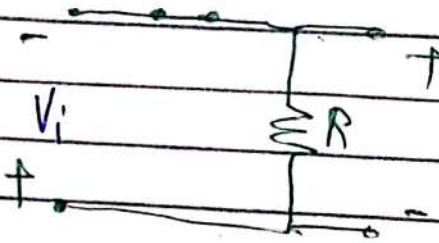
eg H.W.R is a negative clipper.

Example





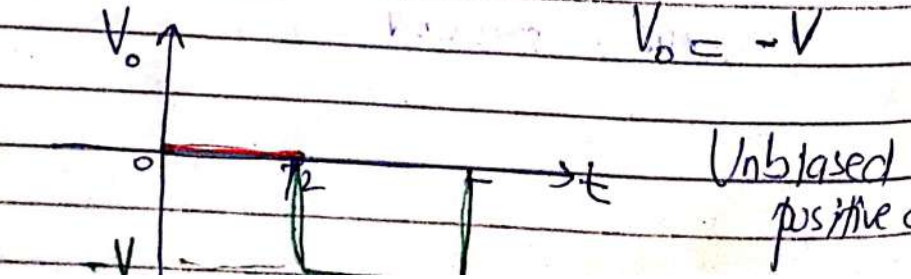
$V_o = 0\ V$



$V_o = V_i$

$V_i = -V$

$V_o = -V$

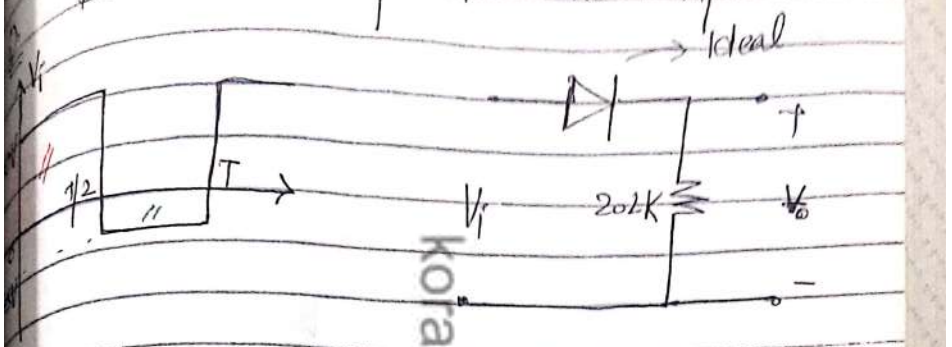


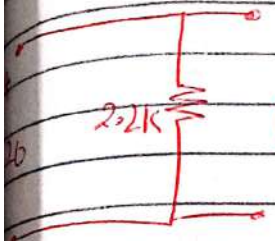
Unbiased series positive clipper.

Unbiased Series Clippers.

Practical diode to be replaced with its barrier potential

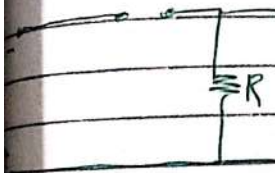
Determine V_o for the shown input.



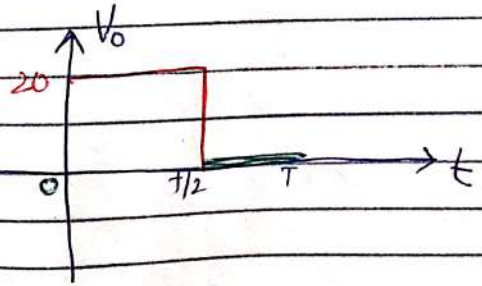


$V_o = V_i$ $\quad 0 \le t < T/2$

$= 20V$

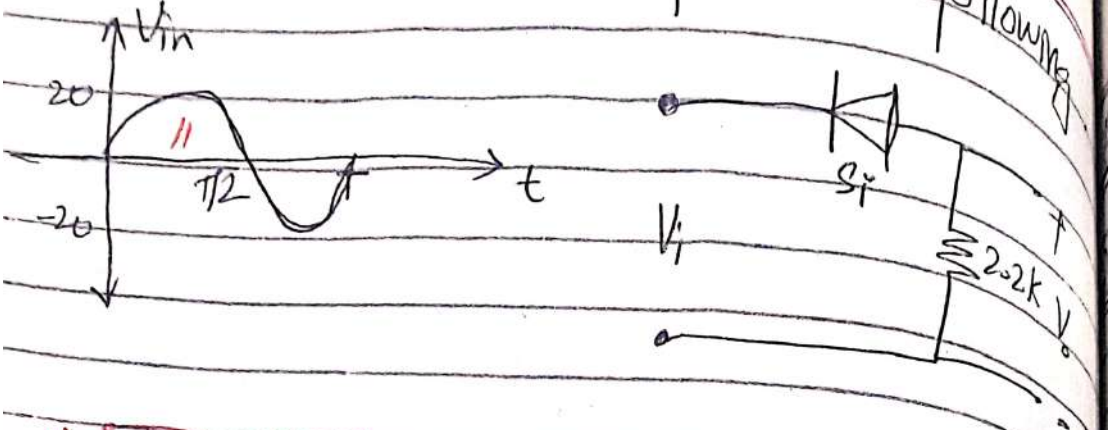


$V_o = 0V$ $\quad T/2 < t \le T$

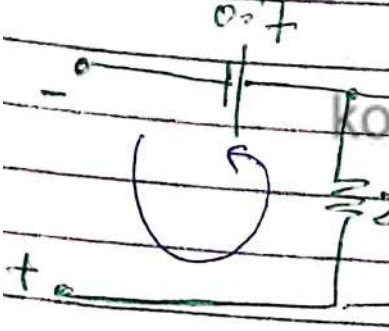


Negative unbiased series clipper

Q2. Delermine V_o for the following.



$V_o = 0\ V$



$V_i + V_o - 0.7 = 0$

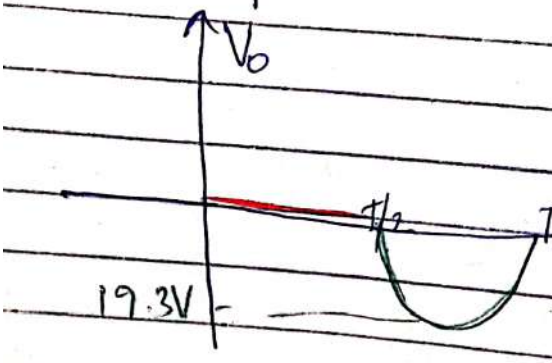
$V_o = -V_i + 0.7$

$= -(20) + 0.7$

$V_o = -19.3\ V$

only 20 not -.

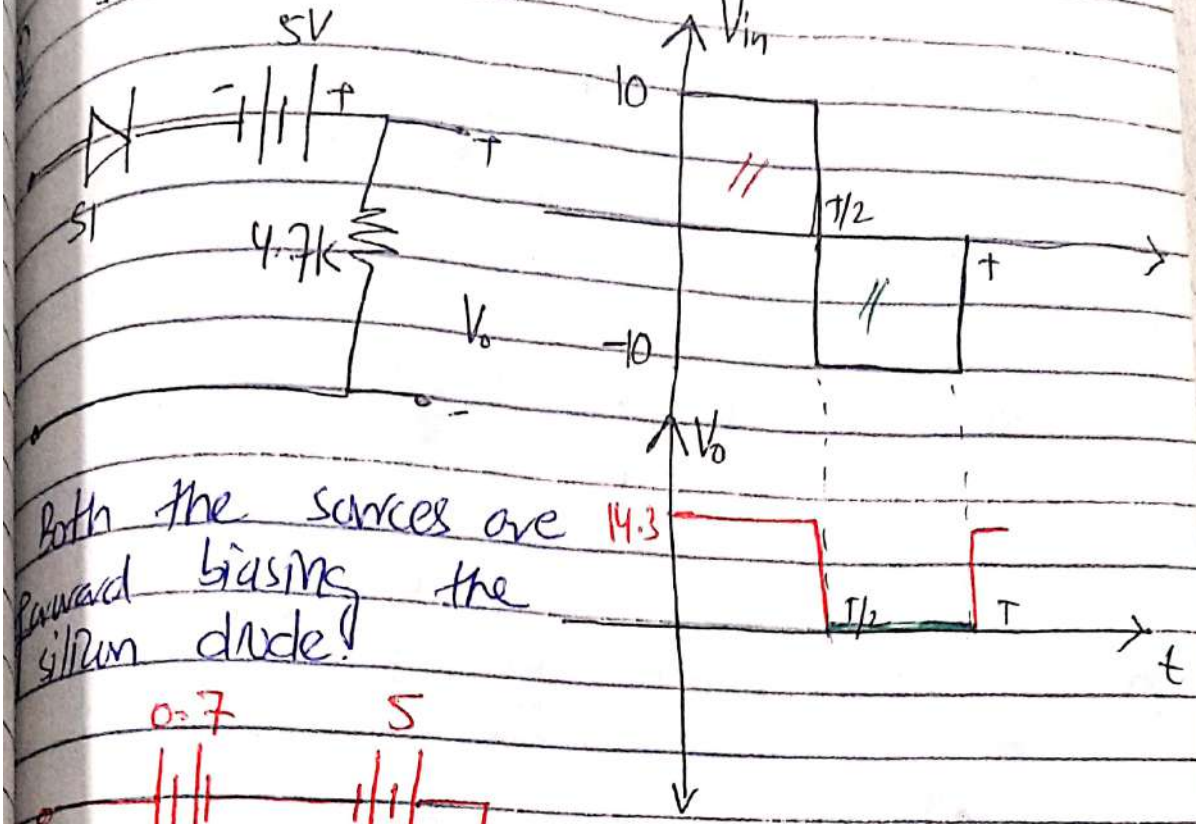
$V_o = 0$ if $V_i < V_b$



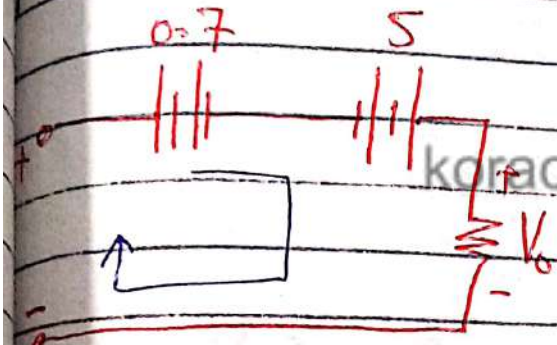
Positive unbiased series clipper.

Biased Series Clipper

Determine V_o



Both the sources are forward biasing the silicon diode!



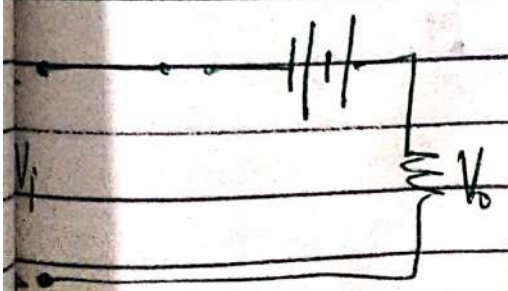
$V_o = V_i - 0.7 + 5V$

$V_i = 10$

$V_o = 14.3\ V$

State of the diode will depend on the greater magnitude voltage source.

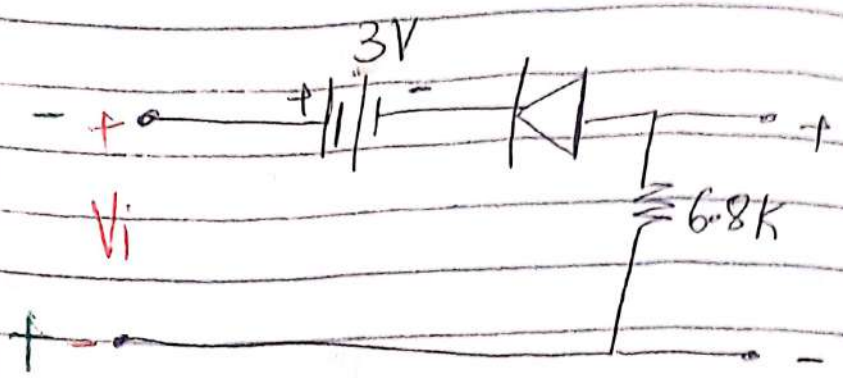
$10 > 5 \Rightarrow$ reverse biased.



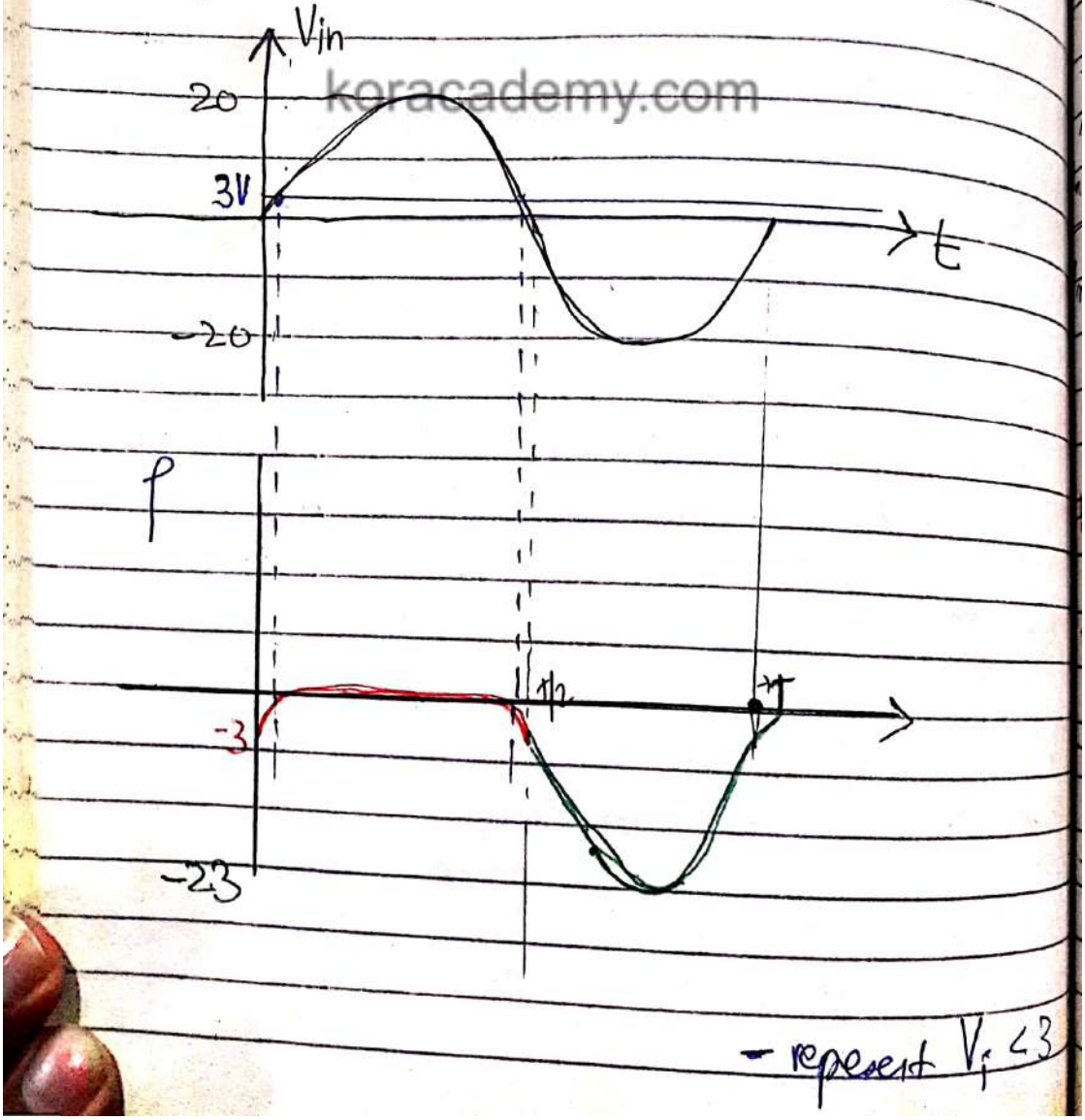
$V_o = 0V$ as there is no flow of current.

Negative clipper.

Q Determine V_o if $V_m = 20V$



in the first the half cycle 3V supply is forward biasing the diode and V_i is reverse biasing it. So till when the V_i is less than 3V the diode will be ~~reverse~~ biased and $V_i > 3V$ → reverse formed



- represent $V_i < 3$

f.B $V_i < 3V$

$V_o = V_i - 3V \Rightarrow V_i = 0 \quad V_o = -3$

$V_i = 3 \quad V_o = 0$

$V_i > 3V$ R.B

$V_o = 0V$

Both sources are forward biasing diode

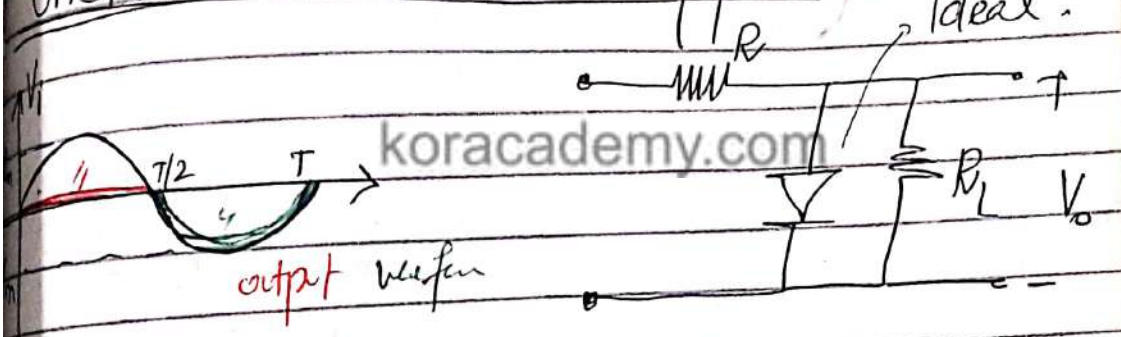
$V_i + V_o + 3V = 0$

$V_o = -V_i - 3V$

$\Rightarrow V_i = 0 \Rightarrow V_o = -3$

$V_i = 20 \Rightarrow V_i = -23V$

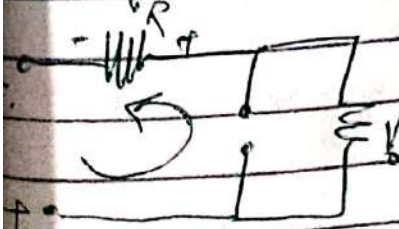
Unbiased Parallel Clippers.



$V_i \geq 0 \rightarrow$ diode forward biased.

$V_o = 0$

current will travel through least resistive path



diode → reverse biased

$V_i + V_o - V_R = 0$

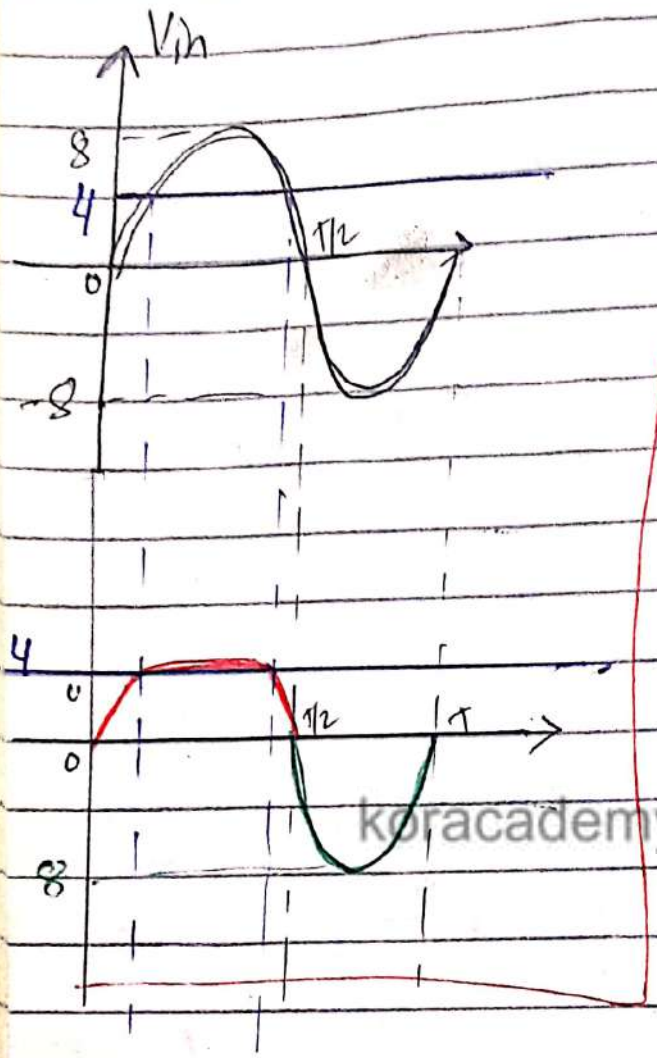
$V_o = -V_i + V_R$

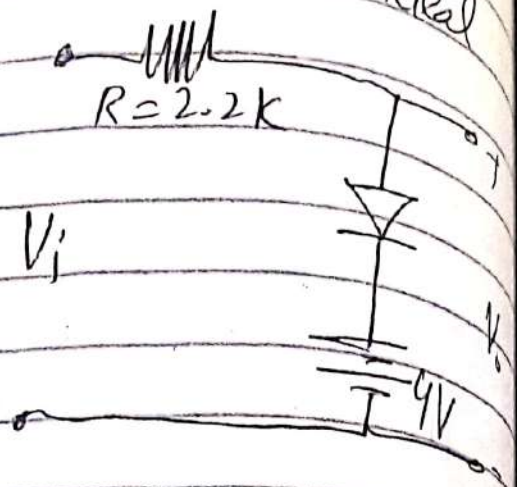
$V_o = -V_i$

As $R << R_L \quad V_o >> V_R$

Biased Parallel Clippers.

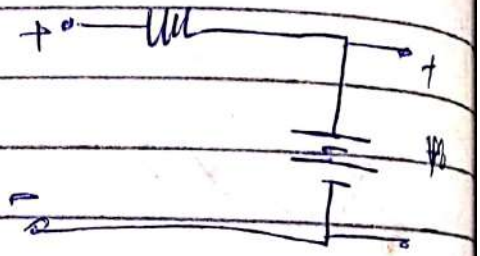
diode → ideal





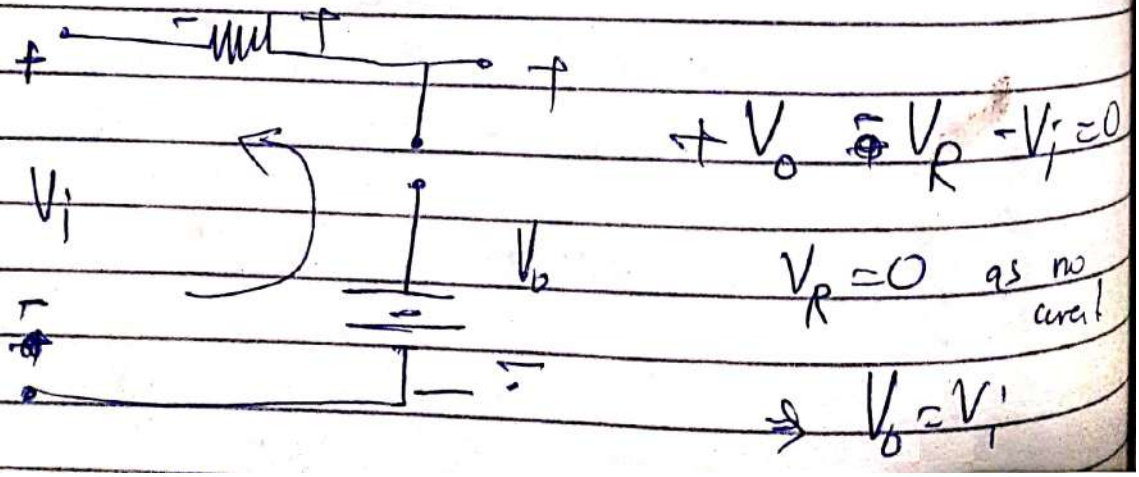
V_i is forward biasing 4V since is reverse biasing

F.B when $V_i > 4V$



$V_o = 4V$

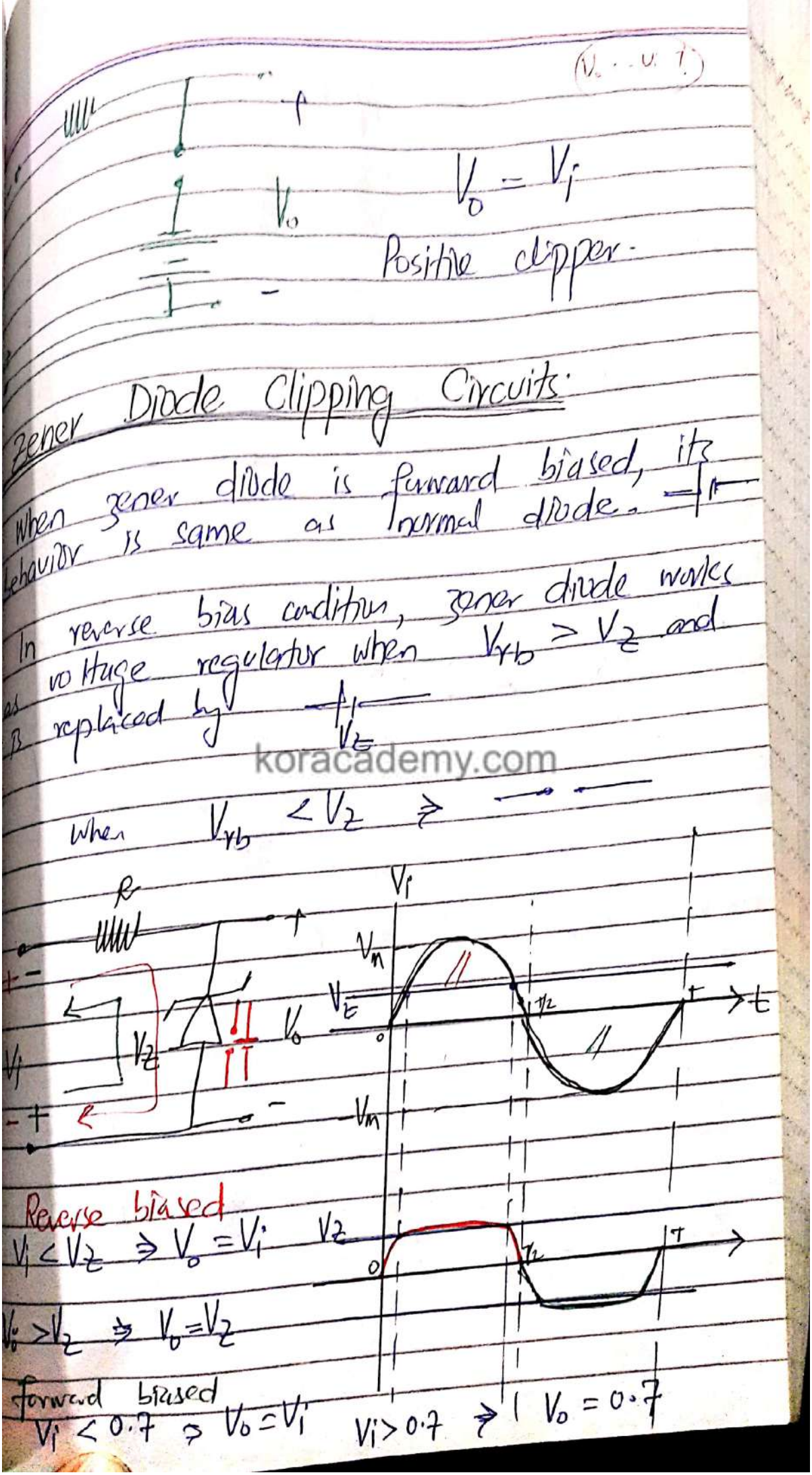
R.B when $V_i < 4V \Rightarrow V_o = V_i$



$+V_o - V_R - V_i = 0$

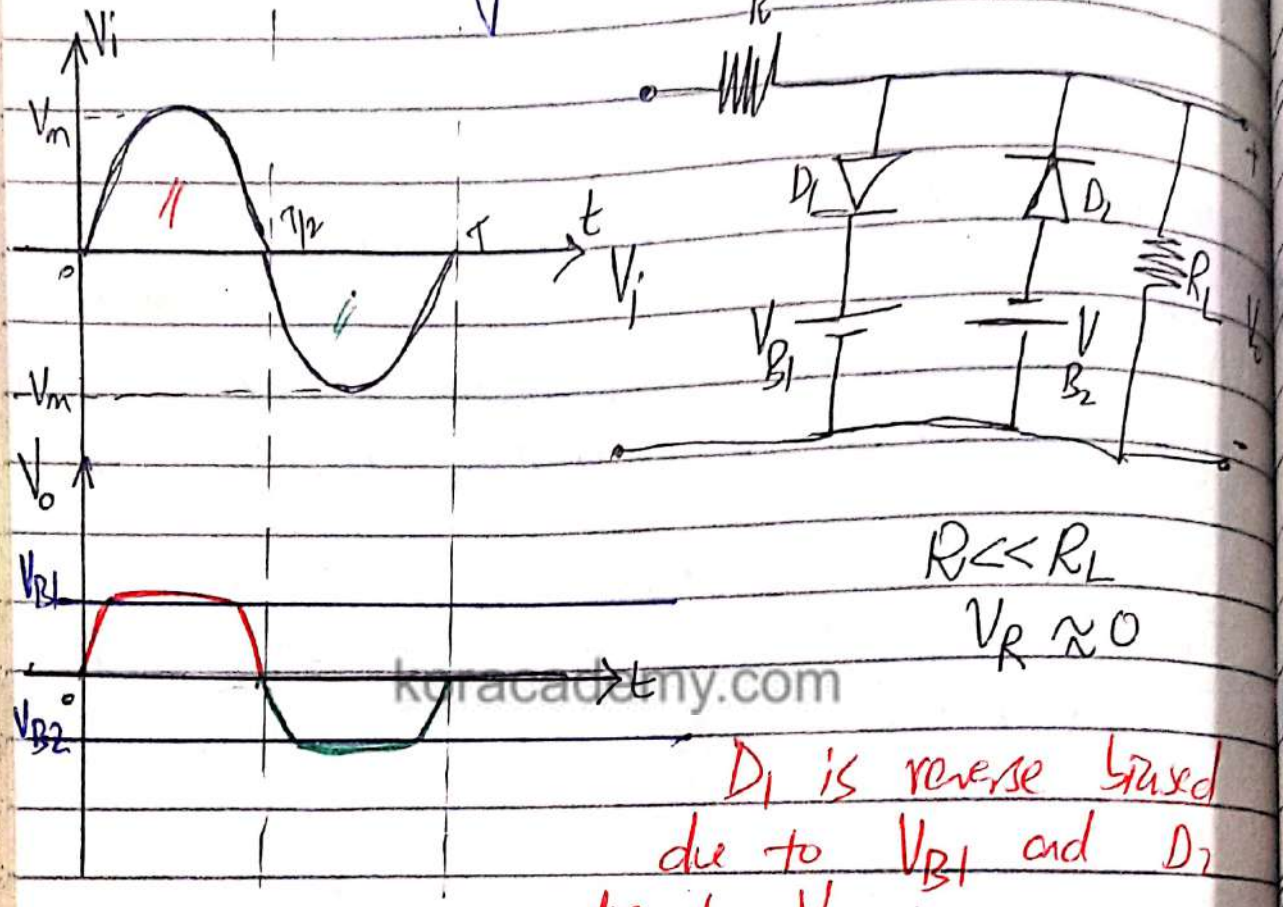
$V_R = 0$ as no current

$\Rightarrow V_o = V_i$



Combination clipper Circuit

It is a combination of biased positive and biased negative clipper circuit.



$R \ll R_L$

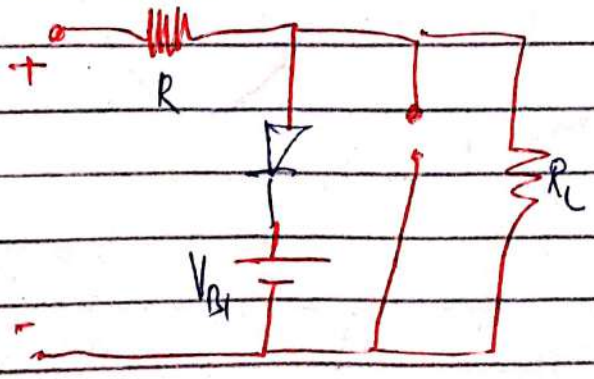
$V_R \approx 0$

D_1 is reverse biased due to V_{B1} and D_2 due to V_{B2}

V_i is f.B D_1 and r.B D_2

(a) $V_i < V_{B1} \Rightarrow D_1$ is r.B

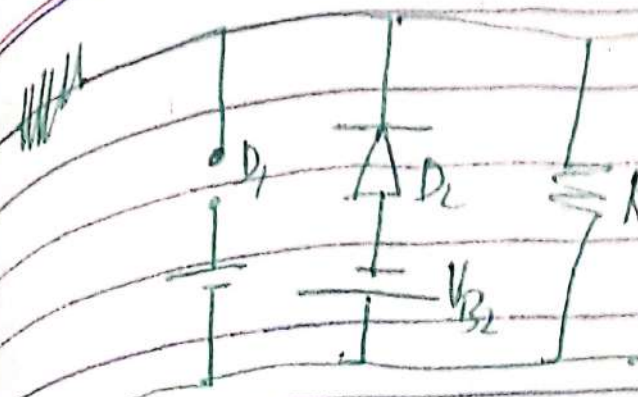
$V_i > V_{B1} \Rightarrow D_1$ is f.B



(a) $\Rightarrow V_o = V_i$

(b) D_1 S.C $D_2 \rightarrow$ O.C

$V_o = V_{B1}$



V_i will F.B D_1

V_i ∫ B D_2 but V_{B2} F.B D_2

$V_i < V_{B2} \Rightarrow R.B \Rightarrow V_o = V_i$

$V_i > V_{B2} \Rightarrow F.B \Rightarrow V_o = V_{B2}$

Both positive and negative cycles clipped.

Transfer Characteristics of Clipper Ckts.

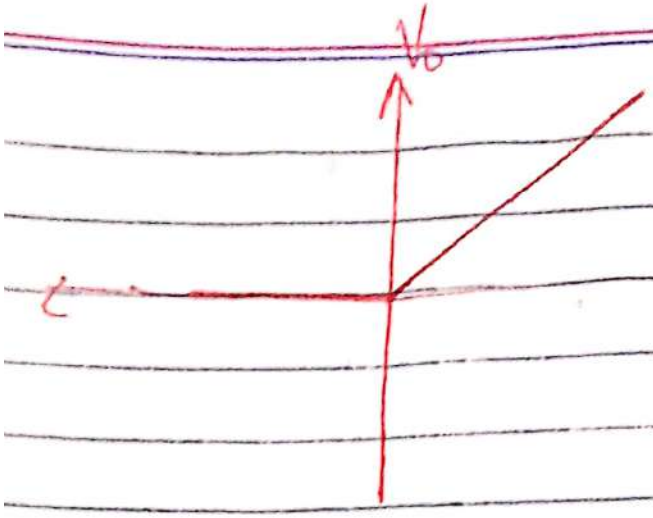
T.C is graph between input voltage and output voltage.

x axis → V_i y axis → V_o

eg

T.C = ?

$$V_o = \begin{cases} V_i & V_i \geq 0 \\ 0 & V_i < 0 \end{cases}$$



$y = x$

$y = mx + c$

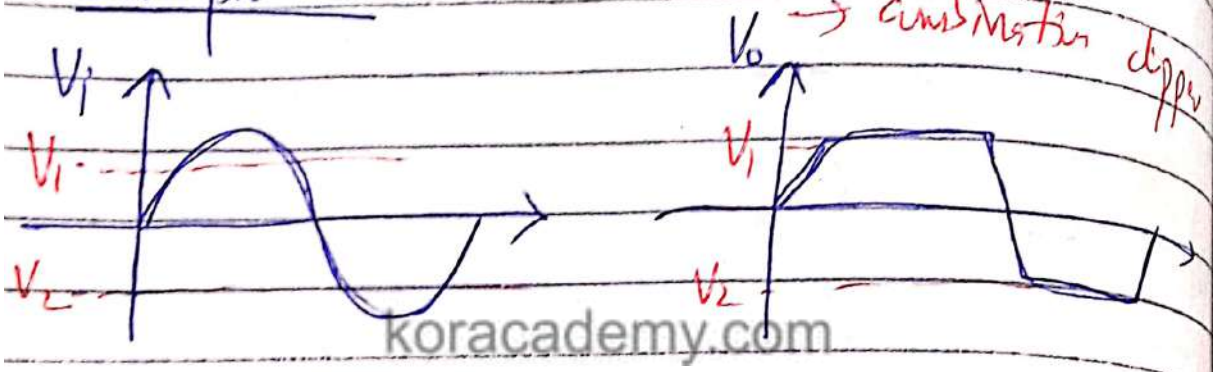
$c = 0$

$m = 1$

$\tan\theta = 1$

$\theta = 45°$

Example 2



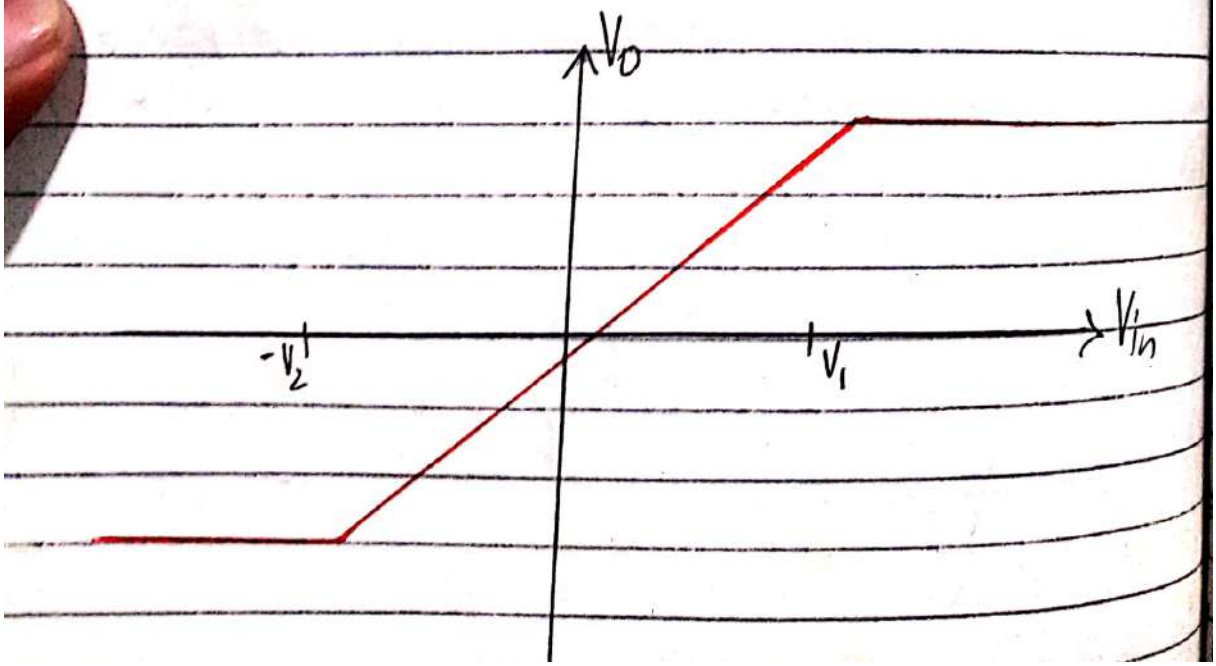
V_o → combination diff

$$V_o = \begin{cases} V_i \\ V_1 \\ -V_2 \end{cases}$$

$-V_2 < V_i < V_1$

$V_i > V_1$

$V_i < -V_2$



Introduction to Clampers.

A clamper is a network constructed a diode, resistor, and a capacitor that shifts the waveform to a different dc level without changing appearance of the applied signal.

OR we can say that;

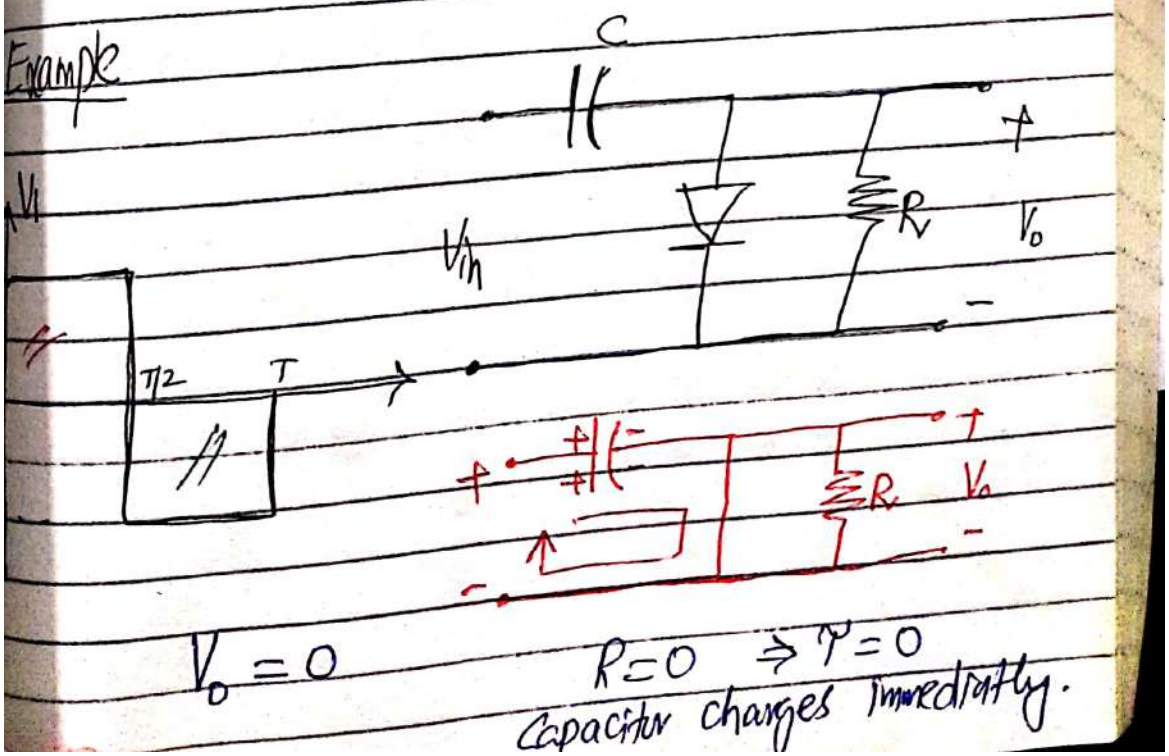
A circuit that places either positive or negative peak of the input signal at a desired dc level.

We have capacitor so definitly there will be charging and discharging. $\tau = RC$

Capacitor must not discharge during the interval when diode is off.

$T/2 \rightarrow$ off $\qquad \tau >> T/2$

Example

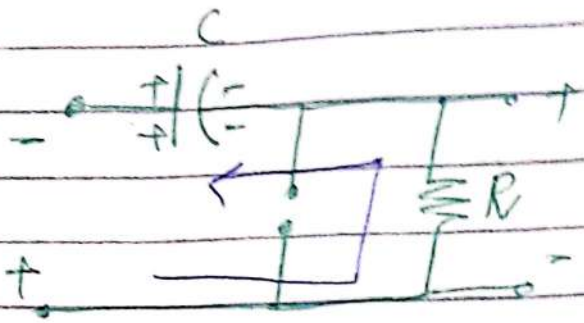


$V_o = 0$ $\qquad R = 0 \Rightarrow \tau = 0$

Capacitor charges immediatly.

$$+V_i - V_c = 0$$
$$V_c = V_i$$

As $V_i = +V \Rightarrow V_c = V$

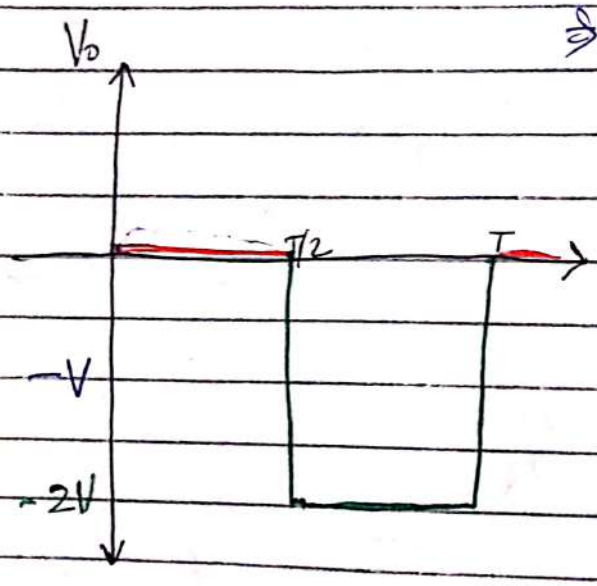


Capacitor will not discharge due to high value of T.

$$+V_i + V_o - V_c = 0$$
$$V_o = -V_i - V$$

$V_i = V \quad V_c = V \Rightarrow V_o = -V - V$

$\Rightarrow V_o = -2V$

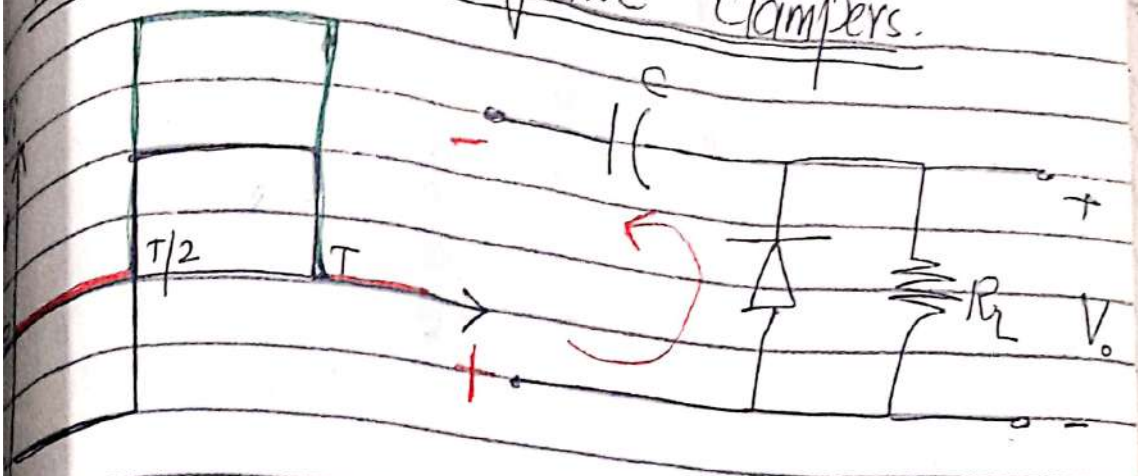


Negative clamper. b/c new dc level is more negative.

NOTE

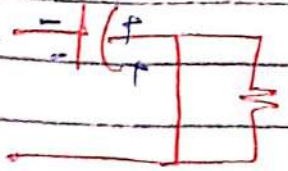
(i) RMS value remains same.
(ii) Peak value changes.
(iii) $\gamma >> T/2$

Positive and Negative clampers.



0 to T/2 $\Rightarrow V_i = -V$ ∴ V_i = +ve.

diode is f.B



$V_o = 0$ b/c no current through R_L. All current will travel through short circuit.

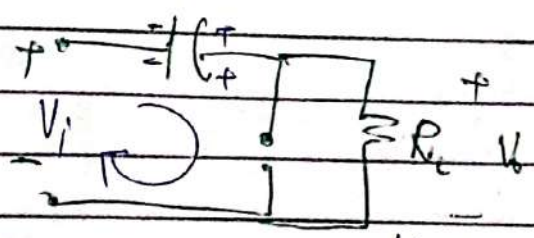
$V_i - V_c = 0 \Rightarrow V_c = V_i = V$

$V_i = -(-V_i) \Rightarrow V_c = V$

(As $-V_i = -V \Rightarrow V_i = V$)

∴ V_i = -ve

T/2 to T



$V_c - V_o + V_i = 0$ KVL

$\Rightarrow V_o = V_i + V_c$

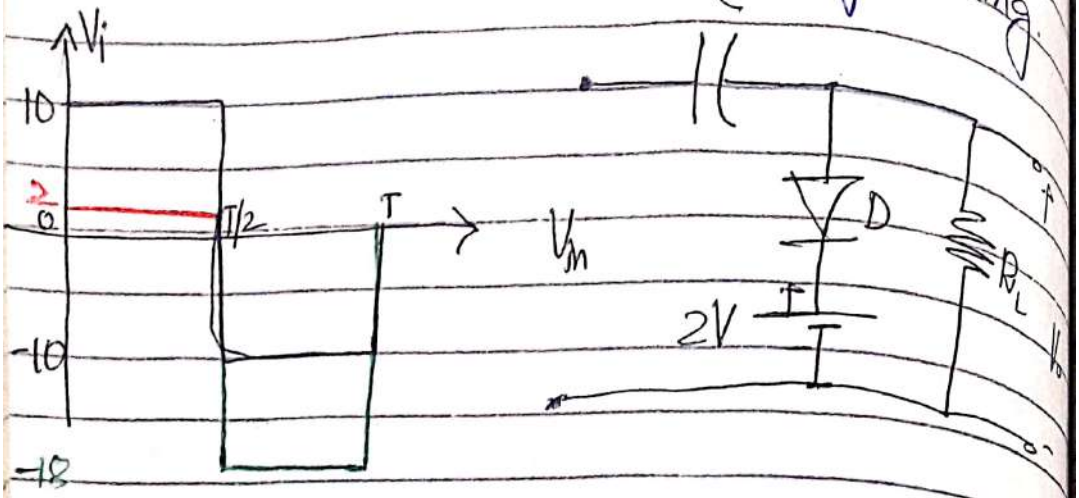
$V_i = V$ $V_c = V$

$\Rightarrow \boxed{V_o = 2V}$

Positive clamper because new dc level is more positive.

Biased Clamper Circuit

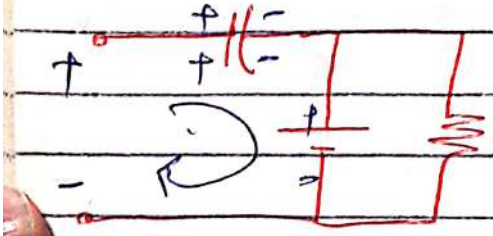
We use biasing in clampers to obtain the additional voltage swing.



0 to T/2 $\rightarrow V_i = 10\ V$ D → f.B

2V → R.B

As V_i 2V → D is f.B → short ckt



$V_o = 2V$

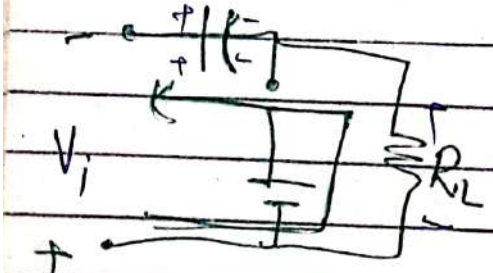
$V_i - V_c - 2V = 0$

$V_c = V_i - 2V$

$\Rightarrow V_c = 8V$

T/2 to T $V_i = -10\ V$

D is r.b



$V_i + V_o + V_c = 0$

$V_o = -V_i - V_c$

$V_o = -(-10) - 8$

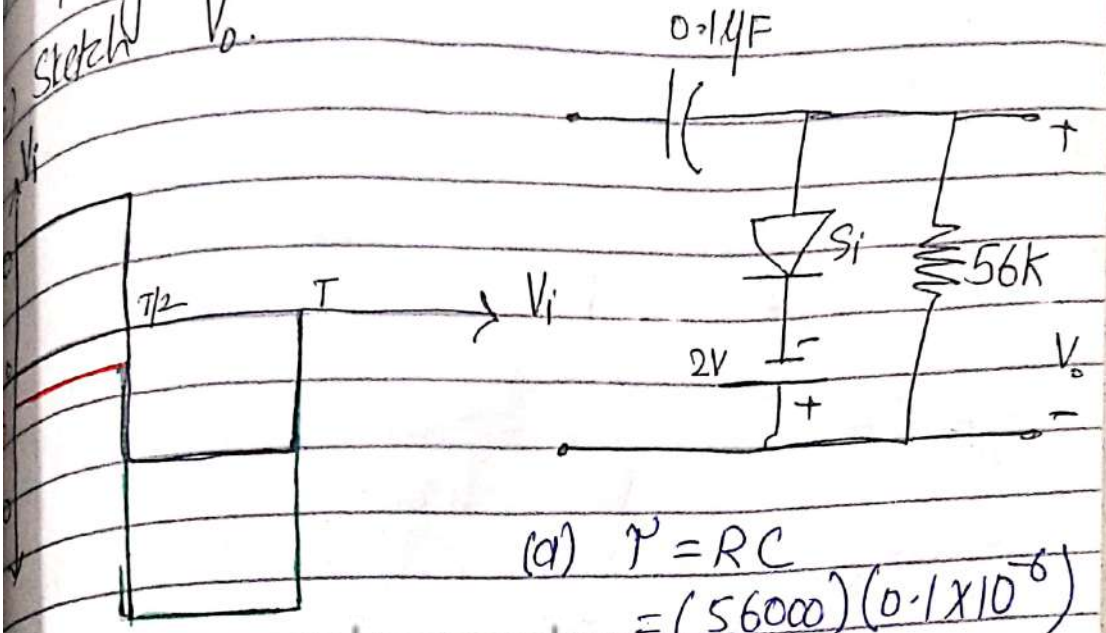
$V_o = -18\ V$

For the network in figure;

a) Calculate 5τ if $f = 1\ kHz$

Compare 5τ to half the period of applied signal.

b) Sketch V_o.



(a) $\tau = RC$

$= (56000)(0.1 \times 10^{-6})$

$\tau = 5.6\ ms.$

$5\tau = 5(5.6m)$

$= 28\ ms$

(b) $T = \frac{1}{f} = \frac{1}{1 \times 10^{-3}}\ s$

$T = 1\ ms$

$\frac{T}{2} = 0.5\ ms$

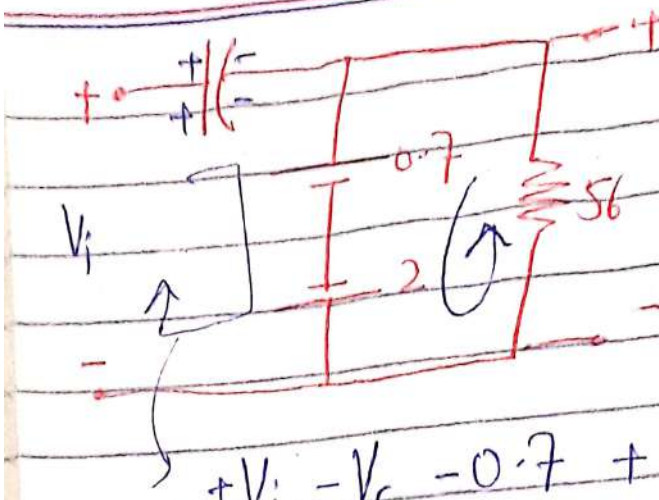
$\Rightarrow 5\tau > T/2$

$28ms > 0.5$

$\frac{5\tau}{T/2} = \frac{28}{0.5} = \frac{56}{0.1}$

$5\tau = 56(T/2)$

(c) $0 \rightarrow T/2$ $V_i = 10V$ $D \rightarrow f.B$



KVL

$-0.7 + 2 + V_o = 0$

$\boxed{V_o = -1.3\,V}$

$+V_i - V_c - 0.7 + 2 = 0$

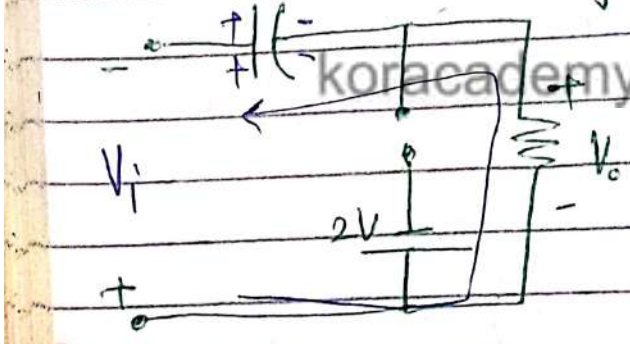
$V_c = 10 - 0.7 + 2$

$V_c = 11.3\,V$

T/2 to T $V_i = -10V$ D is R.B

2V → f biasing

$V_i > 2V$ so D is R.B



$+V_i + V_o + V_c = 0$

$V_o = -V_i - V_c$

$-10 - 11.3$

$\boxed{V_o = 21.3\,V}$

Introduction to Bipolar junction transistor (BJT)

Transistor Invented in December 1947 by John Bardeen, Walter Brattain and William Shockley at Bell labs.

↳ junction version of transistor in 1951.

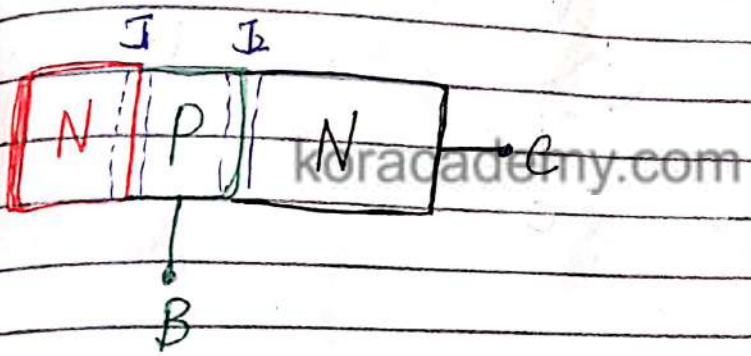
Nobel prize in 1956.

BJT is a three terminal doped semiconductor device and is used in the amplification of weak signals and switching operations.

Physical structure of BJT

Two types NPN and PNP

Three regions in BJT → the largest is the collector, smallest is the base and the medium sized is emitter.



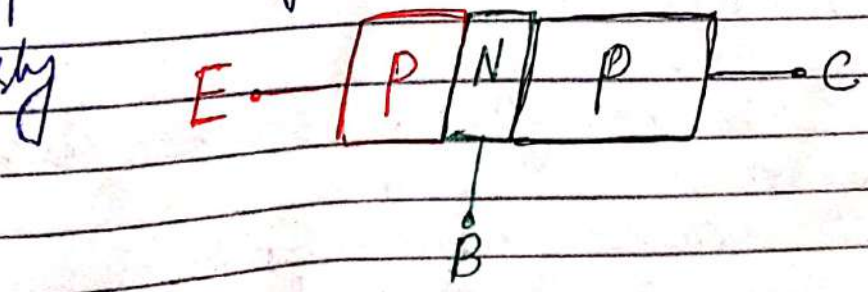
Three regions so two junctions are formed

J_1 → emitter base junction.

J_2 → Collector base junction.

Two depletion regions.

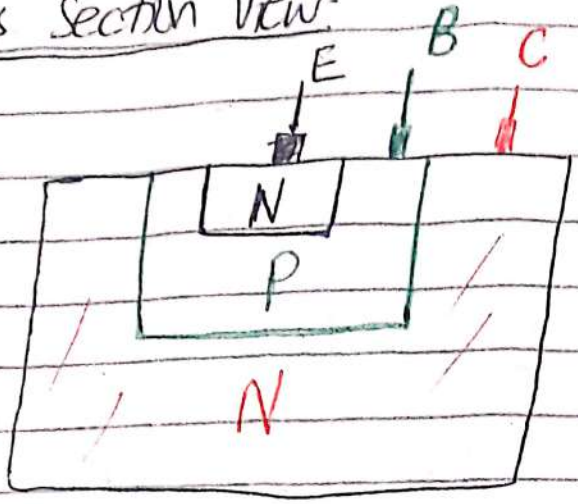
Similarly



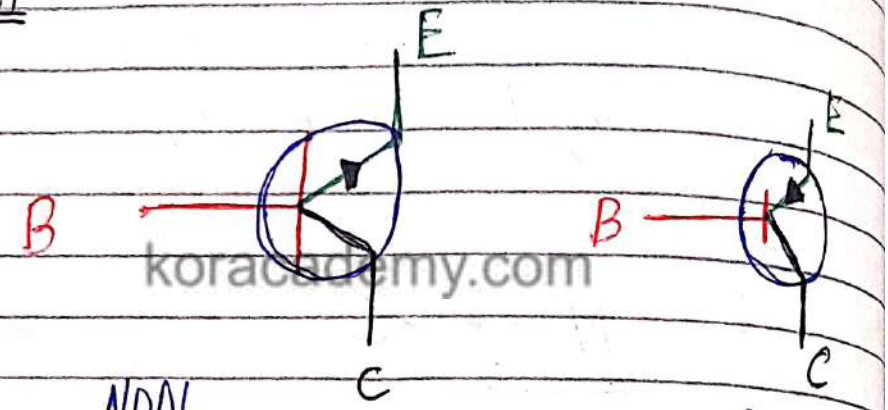
Width → C > E > B

Doping → E > C > B

Cross section View:



Symbol



NPN

n → P
electrons

P current → N

PNP

n → P
electrons

Generally NPN is used.

Two types of charge carriers in transistors;
(i) electrons
(ii) holes

So two types of polarities → hence bipolar.

Transistor → transfer + resistor.
J1 → f.B → very low resistance
J2 → r.B → high resistance.

Weak signal is introduced to low resistance
output is taken at high resistance.
BJT transfers a signal from
low to high resistance.

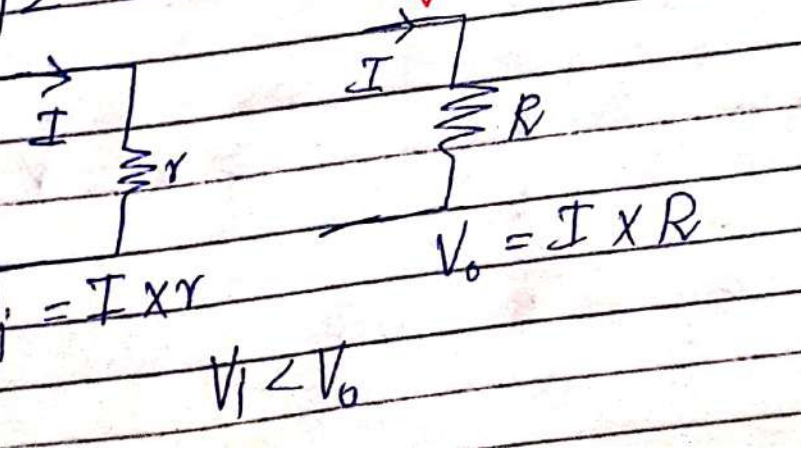
Regions of Operations.

As we have 2 junctions, we have
4 possible ways of biasing the transistor.

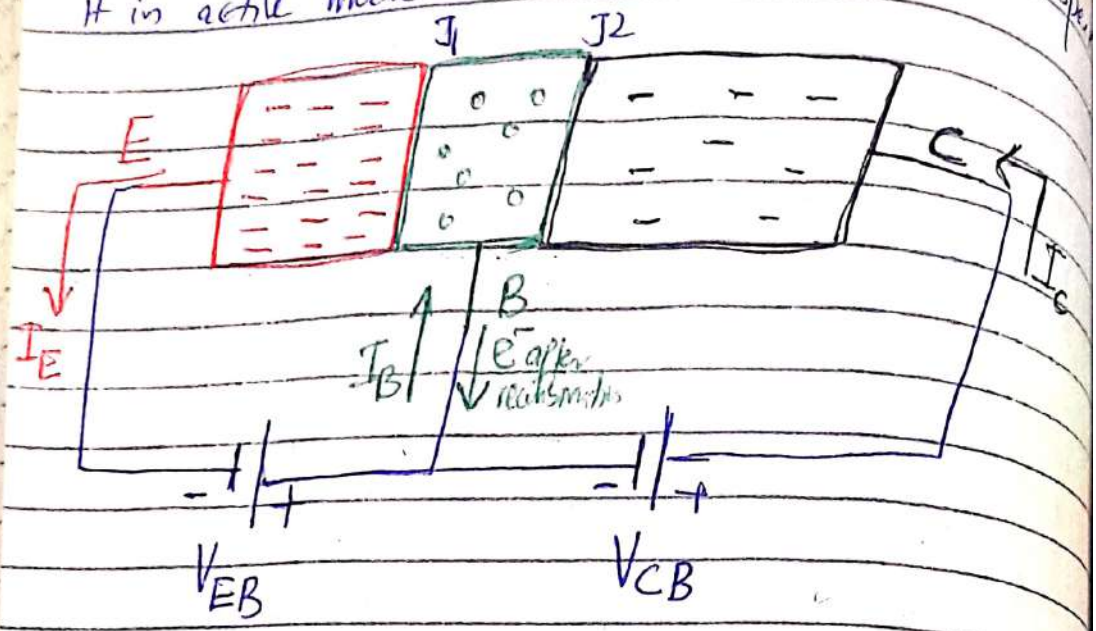
E-B (J_1)	C-B (J_2)	Region of Operation
F.B	R.B	Active → amplifier
F.B	F.B	Saturation → ON mode ↔ closed switch
R.B	R.B	Cut off region → OFF ↔ open ckt
R.B	F.B	Inverted mode rarely used. ← emitter and collector

Working of transistor:

In active mode;
J_1 is F.B → very low resistance $R \approx 0$
J_2 is R.B → very high resistance $R \approx \infty$



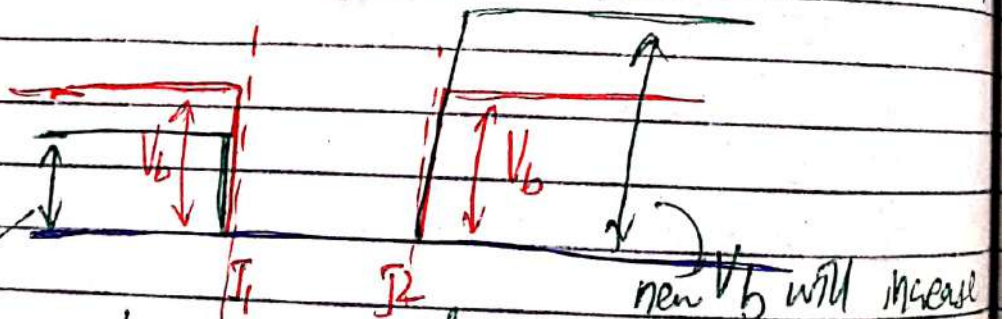
Consider the NPN transistor; we want to operate it in active mode



J1 → F.B J2 → R.B

V_b → barrier potential for J1 and J2 when there is no biasing potential

And we have to analyze what will happen to V_b once we apply the biasing potentials to the transistor.



new barrier potential will decrease due to forward biasing $= V_b - V_{EB}$

new V_b will increase due to R.B $= V_b + V_{CB}$

Base → Very small + lightly doped

Vb at J1 is reduced so electrons from emitter will cross over the junction and very small amount of electrons will recombine in the base (beacuse base is very small) and most electrons will cross the junction J2 due to high velocity ⇒ high KE

Let N electrons entered the base out of which (1−α)N electrons combined with the holes in the base and αN electrons moved to the collector.

2% - 5% electrons combined in the base

Junction J2 is reverse biased so there must be reverse saturation current through J2.

We have minority charge carriers on N side (hole) and on P side (electron) → so leakage (reverse saturation current will be there (I_{CO}) c→collector o→ V_{EB} open circuited

$$I_C = \alpha I_E + I_{CO}$$

Relation b/w emitter current, base current and collector current ?

First find direction of these three currents.

KCL sum of leaving = sum of entering I

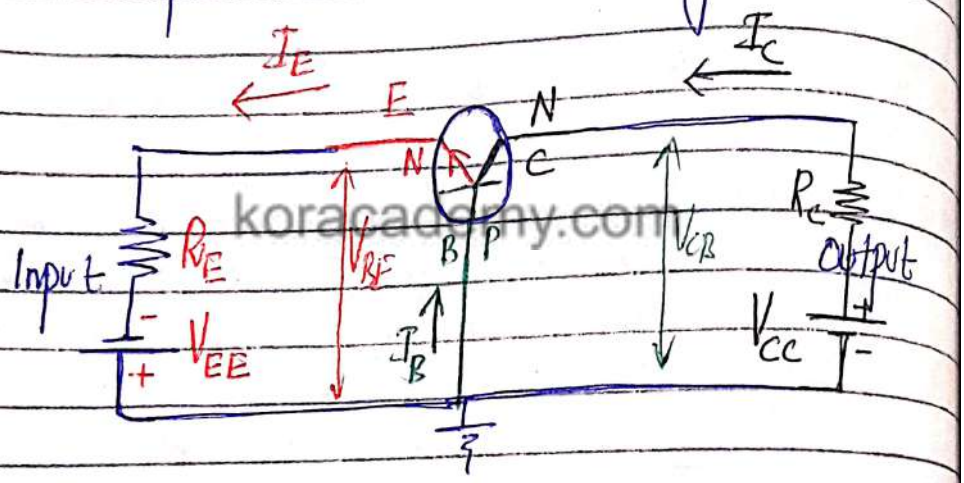
$$I_E = I_B + I_C$$

Three Configurations of transistor:

(i) Common Base
(ii) Common Emitter → mostly used
(iii) Common Collector

① Common Base Configuration

Base is common to the input circuit and output circuit. and is grounded.



Diode → single port
↳ simple IV characteristics

Transistor → two port
↳ we have i/p and o/p char

i/p → plot b/w i/p I (I_E) and i/p V (V_{BE})

o/p → o/p I is I_C and o/p V is (V_{CB})

$V_{BE} = V_{EE}$ $\quad V_{CB} = V_{CC}$

$V_{BE} \neq V_{EB}$ $\quad V_{CB} \neq V_{BC}$ → due to higher and lower potentials.

KCL; $\boxed{I_E = I_B + I_C}$ → for active mode of operation

$$I_C = \alpha I_E + I_{CO} \rightarrow \text{r.s.c}$$

or $$\boxed{I_C = \alpha I_E + I_{CBO}}$$

$$I_E \gg I_{CBO}$$

$$I_C = \alpha I_E$$

$$\boxed{\alpha = \frac{I_C}{I_E}}$$

→ common base current amplification factor

$$\text{gain} = \frac{\text{output}}{\text{input}}$$

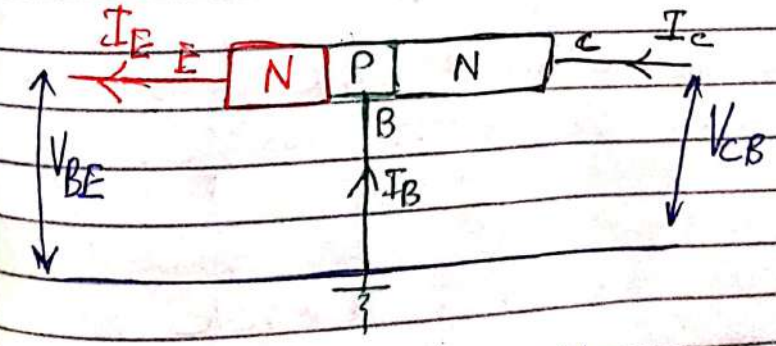
$\alpha = 0.95 - 0.98$

⇒ 95% to 98% emitter current is the collector current. Also there is 2-5% recombination in base.

$$I_B = (1-\alpha) I_E$$

Input Characteristics.

are simply the characteristics of forward biased diode → it is the graphical relation b/w i/p current and i/p voltage for different o/p voltages.



i/p $I = I_E$ i/p $V = V_{BE}$

o/p $I = I_C$ o/p $V = V_{CB}$

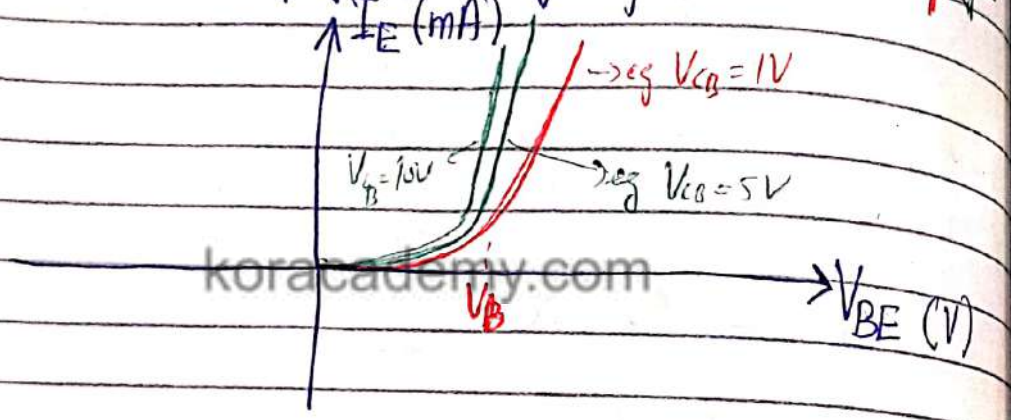
Plot I_E Vs V_{BE} for different values of V_{CB}.

Input characteristics of C.B.T is similar to a F.B diode.

Considering the active mode;

means

We are simply plotting for diode



But what happens to - when we change V_{CB} ?

Early Effect / Base Width modulation

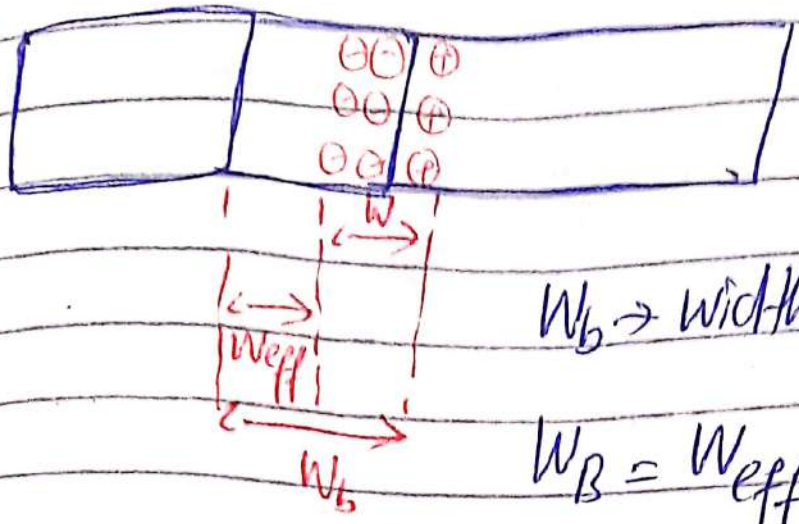
↳ named after James M early.

There is modulation of base width when we increase the output voltage.

R.B ⇒ width of depletion layer decreases ⇒ ↓

⇒ depletion layer will penetrate more in the base region because it is lightly doped.

⇒ +ve immobile ions on collector side
-ve immobile ions on base side. (PN)



W_b → width of base

$W_B = W_{eff} + W$

$W_{eff} = W_B - W$

$V_{CB} \uparrow \Rightarrow W \uparrow \Rightarrow W_{eff} \downarrow \Rightarrow I_E \uparrow$

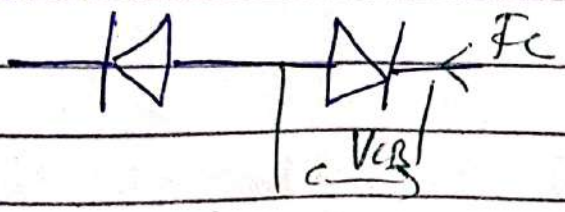
Also chance of recombination also decreases.

$W_{eff} \downarrow \Rightarrow$ Concentration gradient ↑

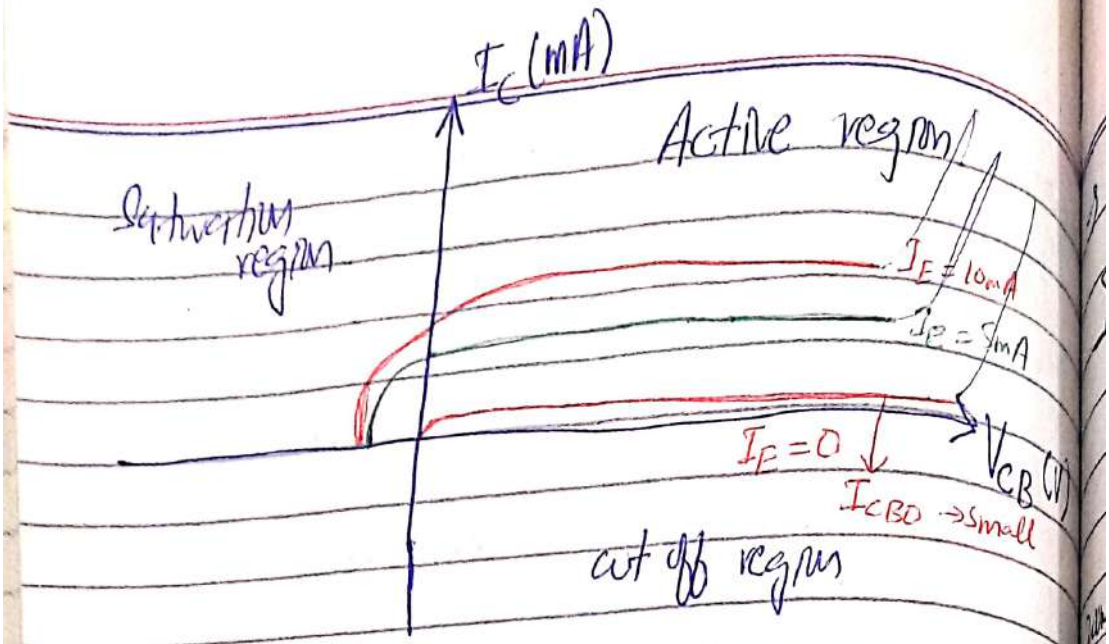
Output Characteristics

O/p current Vs O/p voltage for different input currents.

I_C → output current V_{CB} → output voltage
I_E → Input current



O/P char of C.B.T is simply the R.B char of diode.



As $I_C = \alpha I_E + I_{CBO}$ ↓

$I_C \approx \alpha I_E$

→ Independent of V_{CB}

$I_C \approx I_E$ → ($\alpha = 0.95 - 0.98$) ≈ 1

What will happen if we keep on increasing V_{CB} (reverse bias potential)? → there will be breakdown and current will increase rapidly. (theoretical)

Practically this situation will never arise b/c transistor cannot withstand such high power dissipation.

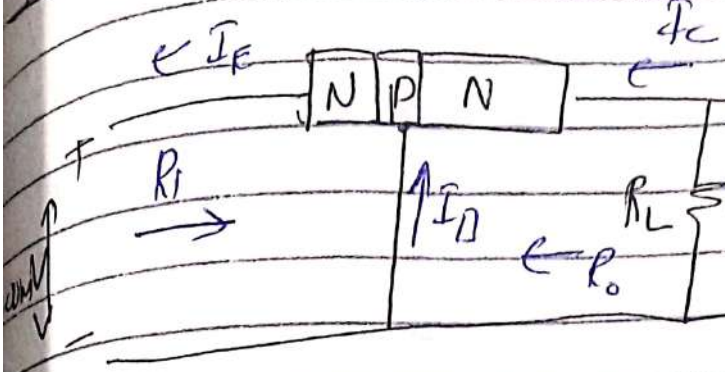
If we insert this graph → similar to reverse bias characteristics of a PN junction diode.

In cut off region both diodes are R.B and transistor will remain OFF → transistor as open switch. ∴ logical 0

In saturation region → both diodes are F.B

s transistor as closed switch, or logical ON.

Transistor Amplifying Action.



$R_i = 20\,\Omega$

slope ↑ = $\frac{1}{R_i \downarrow}$

slope ↓ ≃ 0 R_o ↑

$R_o = 1\,M\Omega$

$V_i = I_i R_i = I_E R_i$

$I_E = \frac{V_i}{R_i} = \frac{200 \times 10^{-3}}{20} \Rightarrow \boxed{I_E = 10\,mA}$

$I_C = \alpha I_E + I_{CBO}$ (↓ ≈ 0)

$I_C \simeq \alpha I_E$ $\quad \alpha = 0.95 - 0.98 \simeq 1$

$I_C \simeq I_E$ $\quad \boxed{I_C = 10\,mA}$

$V_o = I_C R_L = (10\,mA)(5\,k\Omega)$

$\boxed{V_o = 50\,V}$

Voltage Amplification; $A_V = \frac{V_o}{V_i} = \frac{50}{200 \times 10^{-3}}$

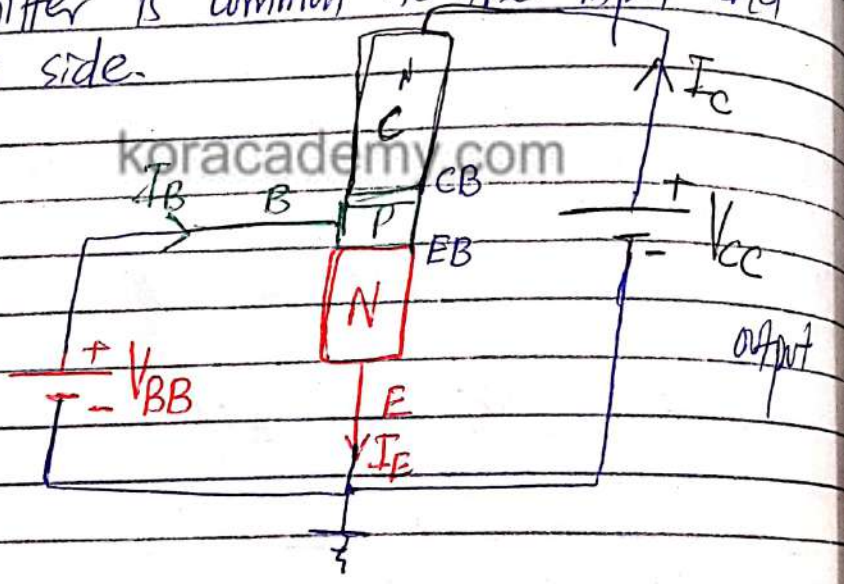
$A_V = 50$ ⇒ the V_o is 50 times V_i

$A_V = 50 - 300$ for C.B.T

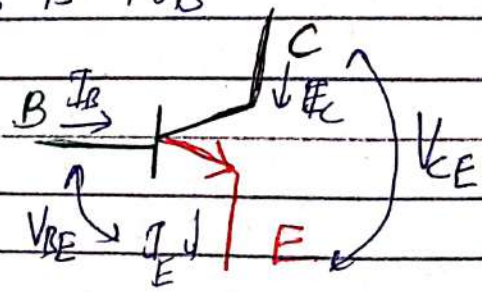
$A_I < 1$ $= \frac{I_C}{I_E} = \frac{\alpha I_E}{I_E}$

② Common Emitter Configuration.

Emitter is common to the input and output side.



Amplifier → active mode ⇒ CB is R.B
EB is F.B



I/P current = I_B I/P Voltage = V_{BE}

O/P curnt = I_C O/P V = V_{CE}

We $I_E = I_C + I_B \rightarrow (1)$

$I_C = \alpha I_E + I_{CBO} \rightarrow (2)$

How output current varies as a function of input current?

In (1) $\Rightarrow I_C = \alpha(I_C + I_B) + I_{CBO}$

$I_C = \alpha I_C + \alpha I_B + I_{CBO}$

$(1-\alpha) I_C = \alpha I_B + I_{CBO}$

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

$$\frac{\alpha}{1-\alpha} = \beta \Rightarrow \beta + 1 = \frac{\alpha}{1-\alpha} + 1$$

$$\beta + 1 = \frac{1}{1-\alpha}$$

$$\Rightarrow \boxed{I_C = \beta I_B + (\beta+1) I_{CBO}}$$

How β changes with change in α.

Case 1 $\alpha = 0.98$ $\beta = \frac{0.98}{1-0.98} = 49$

Case 2 $\alpha = 0.95$ $\beta = \frac{0.95}{1-0.95} = 19$

β is very sensitive to changes in α

$\boxed{50 \leq \beta \leq 400}$

$(\beta+1)I_{CBO} = I_{CEO}$

$I_C = \beta I_B + I_{CEO}$

$I_{CEO} << \beta I_B$

$I_C = \beta I_B$ $\quad \beta = \frac{I_C}{I_B}$

$\beta \rightarrow$ I ~~Gain~~ amplification factor.

eg $I_B = 1mA$ (i/p) $\quad \beta = 100$

$I_C = (100)(1mA)$

$I_C = 100\,mA$

amplification from $1\mu A$ to $100\,mA$

C.E.C works as current amplifier.

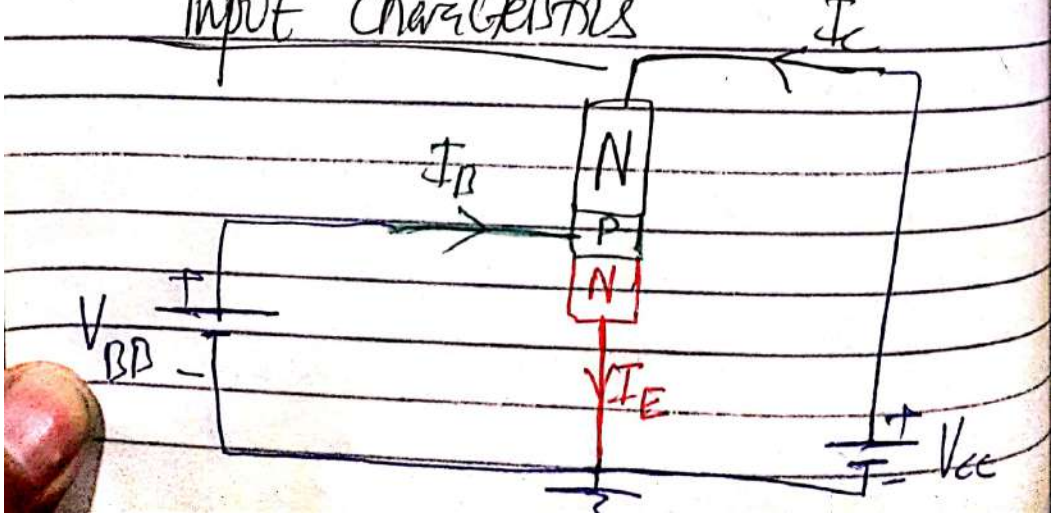
Generally transistor work as voltage amplifier.

In C.B.C $I_C = \alpha I_E + I_{CBO}$

In C.E.C $I_C = \beta I_B + (\beta+1) I_{CBO}$

leakage I in C.E.C has more contribution in C.E.C than in CBC.

Input Characteristics



V_{BB} and V_{CC} → Biasing potentials.

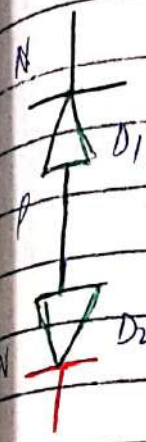
V_{BB} → used to F.B EB Junction.

V_{CC} → used to R.B CB Junction.

I_B → I/P I I_C O/P I.

V_{BE} → I/P V V_{CE} → O/P V

Plot I_B Vs V_{BE} for diffent values of V_{CE}

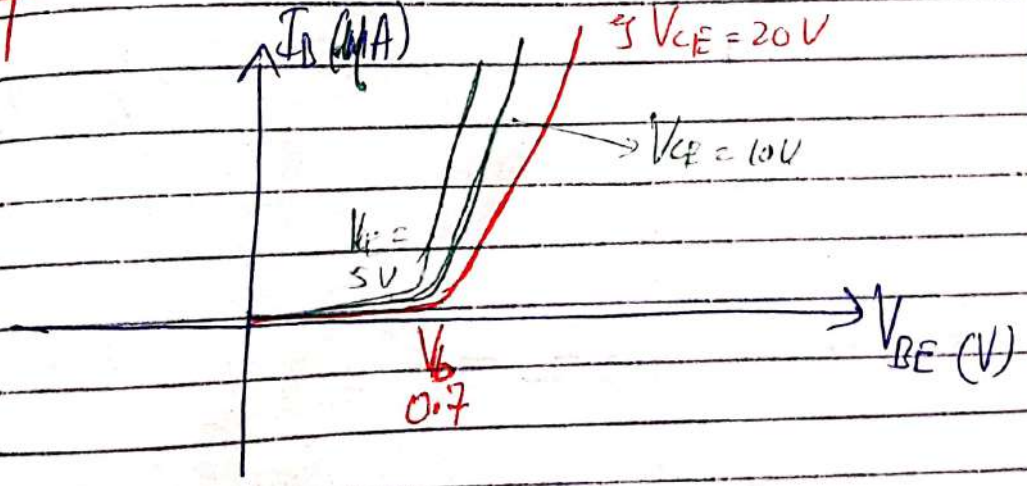


I_B → I through D_2

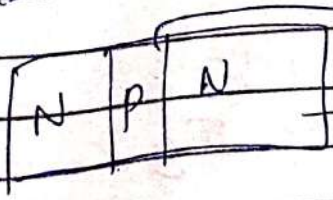
V_{BE} across D_2.

↳ forward biased.

Variation due to V_{CE}?



Base width modulation;



depletion region will penetrate into B.

$W_{eff} = W_B - W$

$V_{CE} = V_{CB} + V_{BE}$

$V_{CE} \uparrow \Rightarrow V_B \uparrow \Rightarrow W \uparrow \Rightarrow W_{eff} \downarrow$

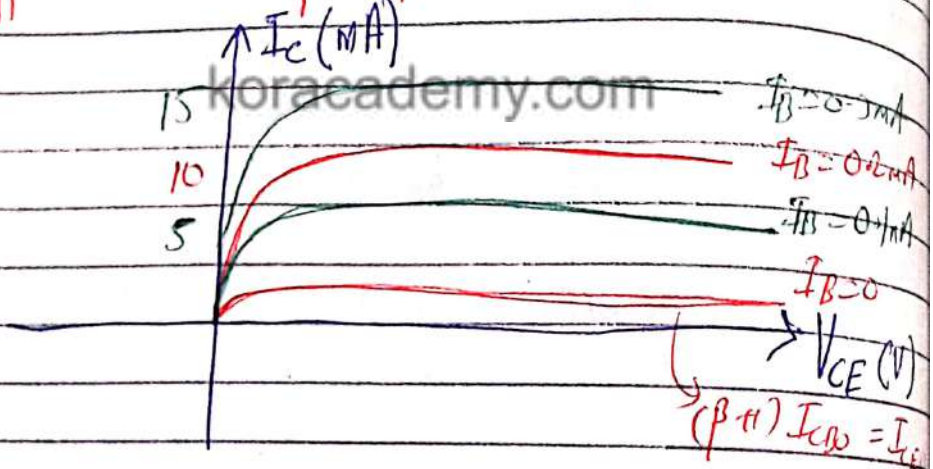
recombination will decrease

$\Rightarrow I_B \downarrow$ (i/p)

$\Rightarrow V_{CE} \uparrow\downarrow = I_B \downarrow\uparrow$

Output Characteristics

o/p $I \rightarrow I_C$ Vs o/p $V \rightarrow V_{CE}$ for different levels of i/p $I \rightarrow I_B$



We know that $I_C = \beta I_B + (\beta+1) I_{CBO}$

when $I_B = 0 \Rightarrow I_C = (\beta+1) I_{CBO}$ → leakage cont.

→ Independent of o/p $V \rightarrow V_{CE}$

depends on i/p cont → I_B

$I_B \uparrow \Rightarrow I_C \uparrow$

$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{10-5}{0.2-0.1} = 50$

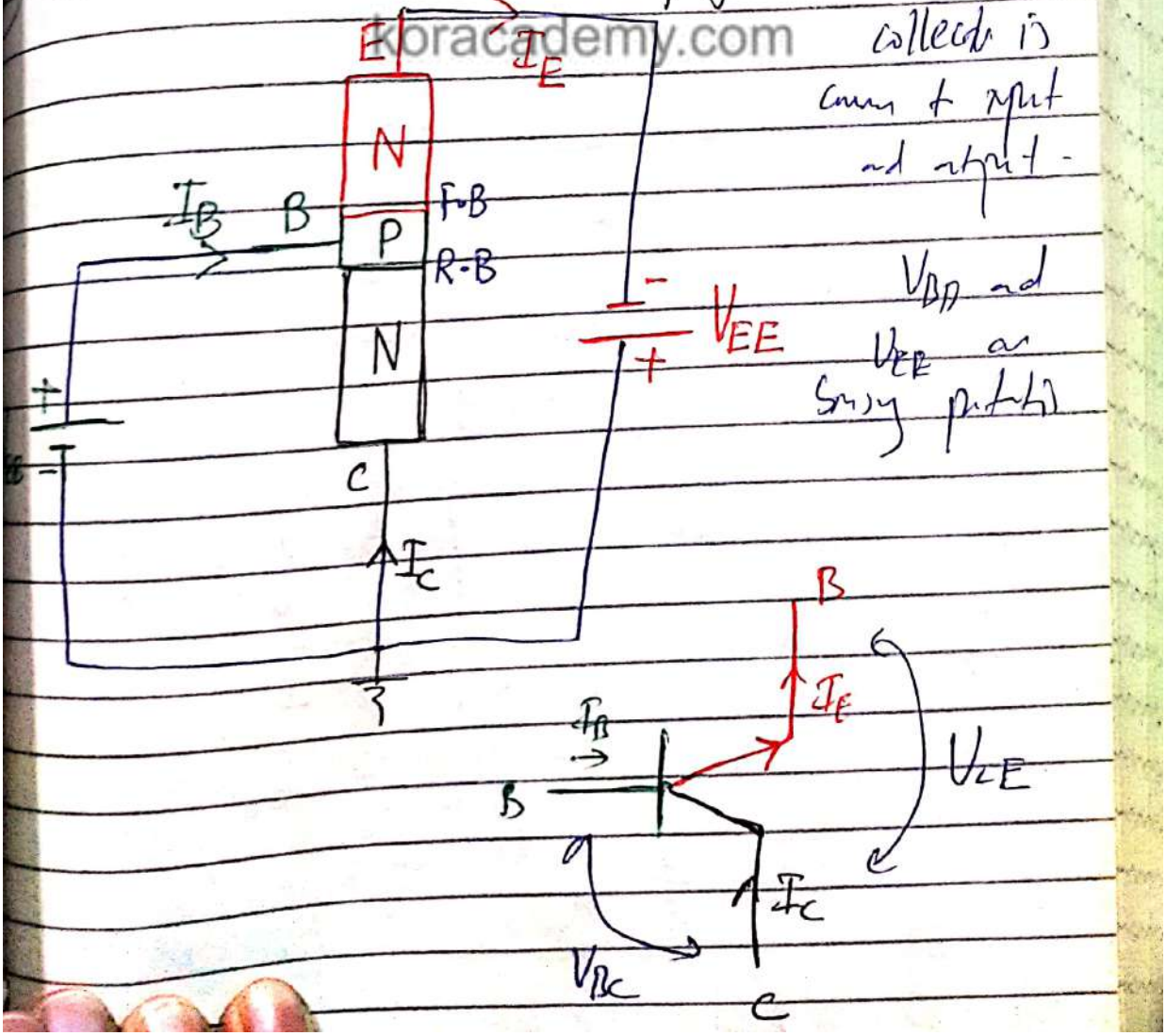
$\beta = 50$ slope $\neq 0$ s/c I_C also depends on V_{CE} due to early effect.

$V_{CE} = V_{CB} + V_{BE}$

$V_{CE} \uparrow \Rightarrow V_{CB} \uparrow \Rightarrow W_{eff} \downarrow \Rightarrow I_B \downarrow$

s/c more electrons from emitter $\in I_C \uparrow$ will be collected at emitter.

Common Collector Configuration



collector is common to input and output.

V_{BB} and V_{EE} are supply potential

$V_{CE} = V_{BE} + V_{BC}$

o/p $I = I_E$ o/p $V = V_{CE}$

i/p $I = I_B$

We know $I_C = \alpha I_E$

$I_C \simeq I_E$

↳ plot I_C Vs V_{CE} ⇒ o/p of C.E.T = o/p Charcti of C.E.T

Current Amplification factor in C.E.T is denoted by γ.

$$\gamma = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta \text{output } I}{\Delta \text{input } I}$$

$I_C = \alpha I_E + I_{CBO} \rightarrow (2)$

$I_E = I_C + I_B \rightarrow (1)$

How I_E varies as function of I_B?

$I_E = \alpha I_E + I_{CBO} + I_B$

$(1-\alpha) I_E = I_B + I_{CBO}$

$$I_E = \frac{1}{(1-\alpha)} I_B + \frac{1}{(1-\alpha)} I_{CBO}$$

$$\boxed{I_E = \gamma I_B + \gamma I_{CBO}}$$

Relationship B/w α, β and γ

α → $\alpha_{dc} = \frac{I_C}{I_E}$ — α → Amplification factor in C.B.C

→ $\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E}$ | V_{CB} = constant

β → $\beta_{dc} = \frac{I_C}{I_B}$ — β → amplification factor in C.E.C

→ $\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$ | V_{CE} = constant

γ → $\gamma_{dc} = \frac{I_E}{I_B}$ — γ → amplification factor in C.C.C

→ $\gamma_{ac} = \frac{\Delta I_E}{\Delta I_B}$ | V_{CE} = constant

We know that $I_E = I_C + I_B$

Dividing by I_B

$$\frac{I_E}{I_B} = \frac{I_C}{I_B} + \frac{I_B}{I_B}$$

$$\boxed{\gamma = \beta + 1}$$

& $\beta = \frac{\alpha}{1-\alpha} \Rightarrow \boxed{\gamma = \frac{1}{1-\alpha}}$

$$\gamma = \beta + 1 = \frac{1}{1-R}$$

ELECTRONICS I (FINAL)

DC Biasing of transistors

The analysis of transistor as an amplifier requires the knowledge of both dc and ac respance of the system.

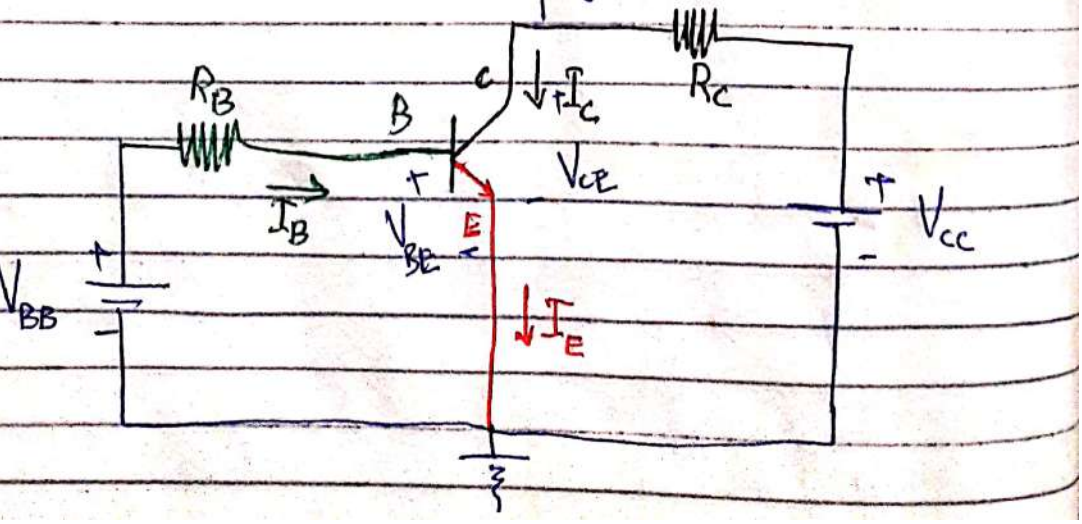
DC and ac analysis can be done separately, but the parameters chosen in dc analysis will effect the ac response and also vice versa.

Once the desired dc current and voltage levels are defined, we can construct a network that will establish the desired operating point.

Biasing? the process of applying external dc voltages to select an appropriate operating point.

To use transistor as an amplifier, it is biased in the active region.

Here we are using NPN transistor with a common emitter configuration.



Emitter is common to both input and output.

Input voltage $= V_{BE}$ Input current $= I_B$

output voltage $= V_{CE}$ Output current $= I_C$

We want to amplify a weak input signal without any distortion

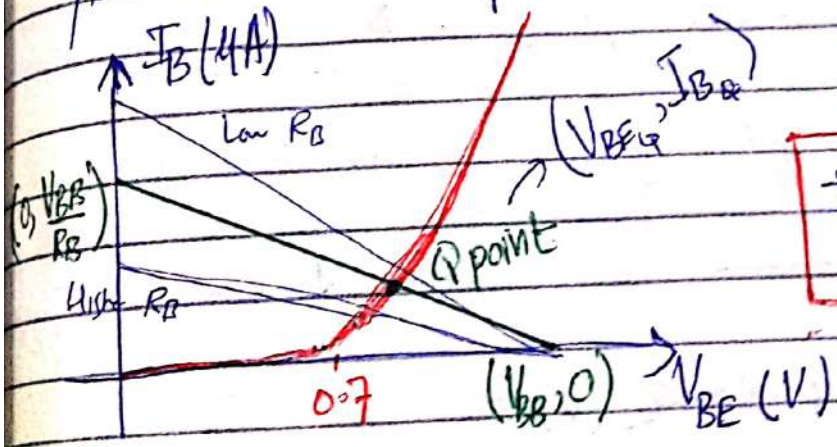
Operating points ?

Transistors are two port devices.

(1) I/P op point:

the cordinates obtained by the intersection of load line with the transistor i/p characteristic for the particular value of o/p voltage V_{CE}.

I/P characteristics of Comm Emitter.



KVL to i/p loop.

$$+V_{BB} - I_B R_B - V_{BE} = 0$$

$V_{BE} = x$ axis

$I_B = y$ axis

Minimum two points required for straight line (load line)

$V_{BE} = 0 \Rightarrow I_B = V_{BB}/R_B$ $P_1 = (0, V_{BB}/R_B)$

$I_B = 0 \Rightarrow V_{BE} = V_{BB}$ $P_2 = (V_{BB}, 0)$

If we increase the o/p voltage the curve will shift right and if we decrease the o/p voltage the curve will shift to left.

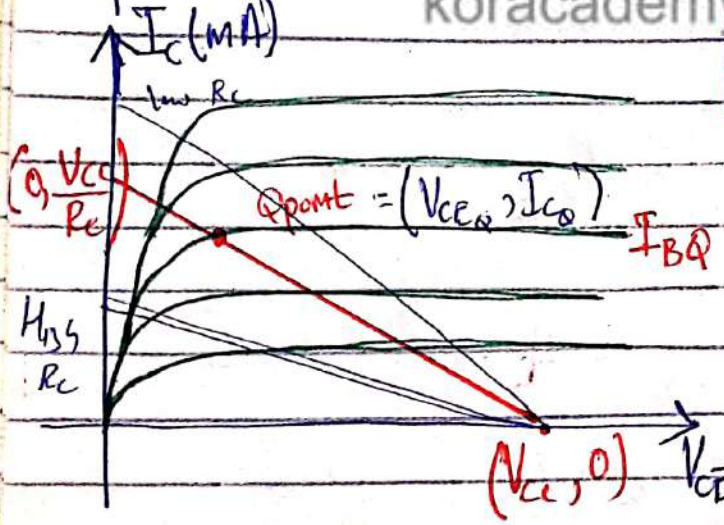
We can also change the Q point by changing the resistance R_B.

$$\text{slope} = -\frac{1}{R_B}$$

(ii) Output operating point

The intersect of load line with the transistor output characteristics for particular value of base current (I_B) gives the operating point.

Output Characteristics



KVL to O/P loop

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Two points?

$V_{CE} =$ y axis

$I_C =$ y axis.

$$V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C} \qquad P_1 = \left(0, V_{CC}/R_C\right)$$

$$I_C = 0 \Rightarrow V_{CE} = V_{CC} \qquad P_2 = (V_{CC}, 0)$$

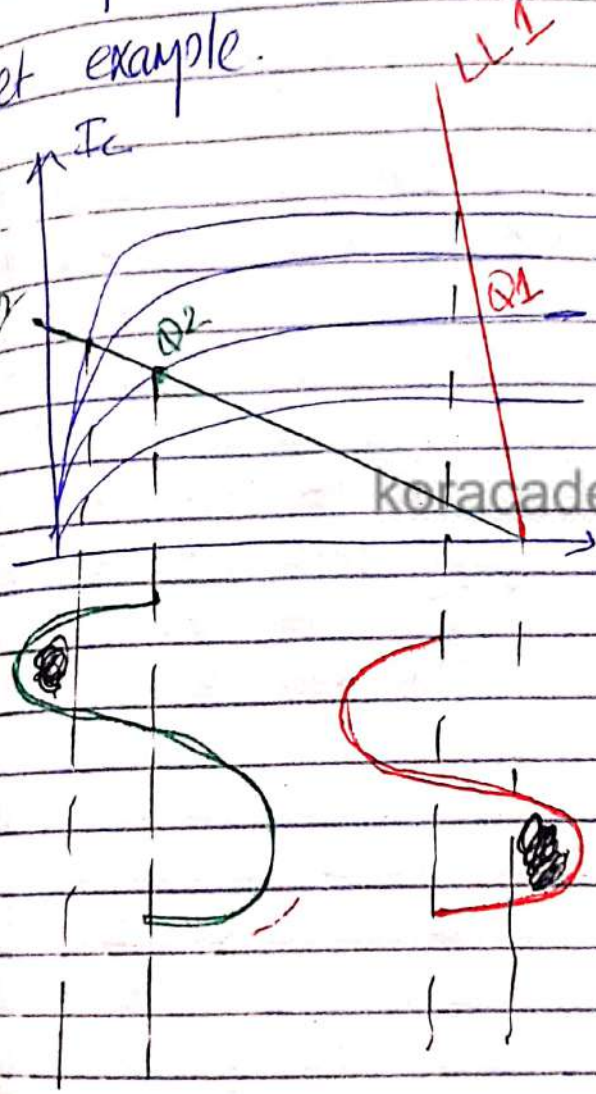
Operating point will change by changing base current I_B and also by changing R_C.

$$\text{slope} = \frac{-1}{R_c}$$

Why setting of operating point is very important?

If op point is near to saturation or cutoff region, we will not have distortionless output signal.

let example.



the shaded regions are clipped off.

When op point is near to saturation region → -ve portion is clipped.

When near to cut off region → +ve portion is clipped.

Operating point → best → in centre of active region.

Collector current may change due to;

(i) change in β value.

As $I_C = \beta I_B$

(ii) change in temperature.

$I_C = \beta I_B + (\beta+1) I_{CBO}$

I_{CBO} → due to minority charge carriers → due to temperature

Temp ↑ → MCC ↑ → I_{CBO} ↑

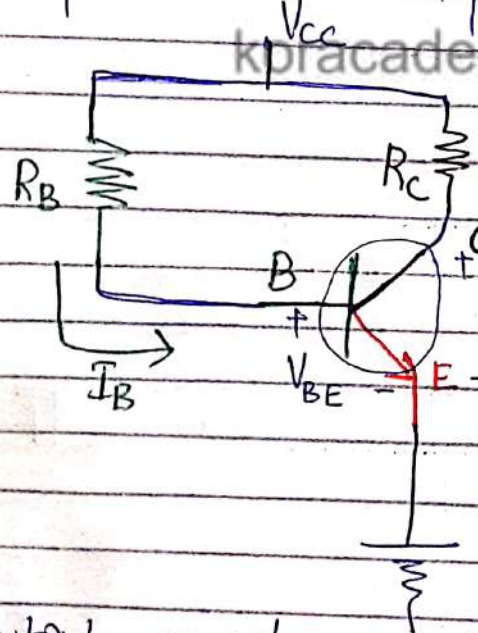
⇒ I_C ↑

Fixed Biased Configuration

Also known as base bias configuration

V_{CC} → biasing potential

↳ potential at point.



Emitter base junction is forward biased by V_{CC}. Collector base junction is reverse biased by V_{CC}.

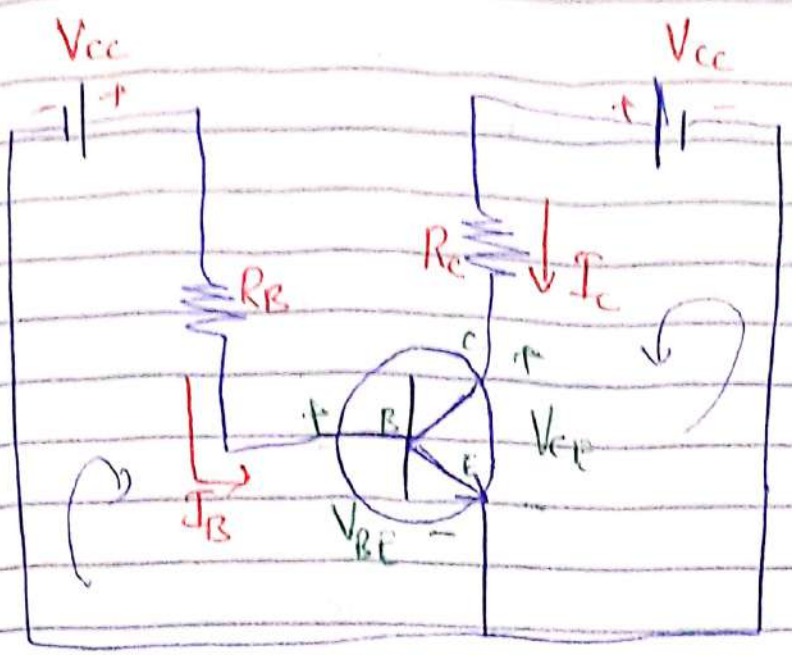
Output current I_C = ? V_{CE} = ? (o/p voltage)

Representing V_{CC} as potential difference and redrawing the above circuit.

KVL to input loop.

$V_{CC} - I_B R_B - V_{BE} = 0$

$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$



As $I_C = \beta I_B$ $\quad V_{BE} = 0.7$ Si
$= 0.3$ Ge

$$\Rightarrow \boxed{I_C = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right)}$$

↓ it is the voltage across the forward biased diode.

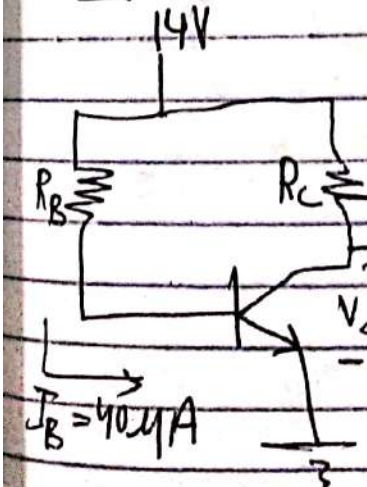
o/p voltage (V_{CE})

KVL to o/p loop

$+V_{CC} - I_C R_C - V_{CE} = 0$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

Q. For the following fixed bias configuration,



$\beta = 80$ (a) I_C (b) R_C
(c) R_B (d) V_{CE}

$V_C = 6V$ $\quad V_{CC} = 14V$

$I_B = 40\mu A$ $\quad \beta = 80$

$V_C = 6V$

(a) $I_C = \beta I_B = 80(40\mu)$

$\Rightarrow I_C = 3.2\,mA$

(b) KVL to o/p loops. (point potential)

$14 - I_C R_C = 6V$

$R_C = \frac{14-6}{3.2m}$

$\Rightarrow R_C = 2.5 k\Omega.$

(c) R_B KVL to i/p loop.

$14 - I_B R_B - V_{BE} = 0$

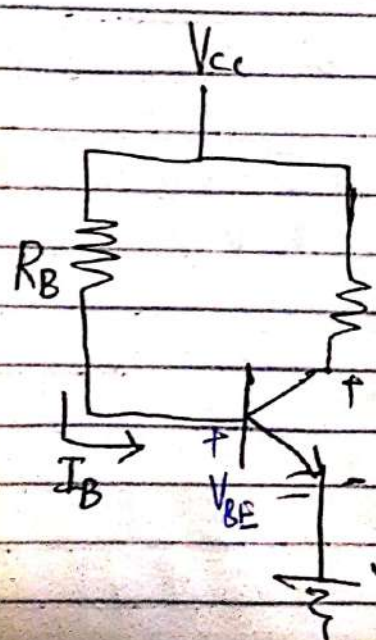
$R_B = \frac{14-0.7}{40\mu} \Rightarrow R_B = 332.5 k\Omega.$

(d) $V_{CE} = V_C - V_E$

$= 6 - 0 \Rightarrow V_{CE} = 6V$

Two coupling capacitors are replaced by open circuit in dc analysis.

Q. Determine I_C, V_{CC}, β, R_B



$R_C = 2.7 k\Omega \quad I_B = 20\mu A$

$I_E = 4mA \quad V_{CE} = 7.2V$

(a) $I_E = I_C + I_B$

$\Rightarrow I_C = I_E - I_B$

$= 4m - 20\mu$

$\Rightarrow I_C = 3.98 mA$

$I_C \approx I_E$

(b) KVL to o/p loop

$$V_{CC} - I_C(2.7k) - 7.2 = 0$$

$$V_{CC} = (2.7k)(3.98m) + 7.2$$

$$\Rightarrow V_{CC} = 17.9V$$

(c) $$\beta = \frac{I_C}{I_B} = \frac{3.98m}{20\mu} \Rightarrow \beta = 199$$

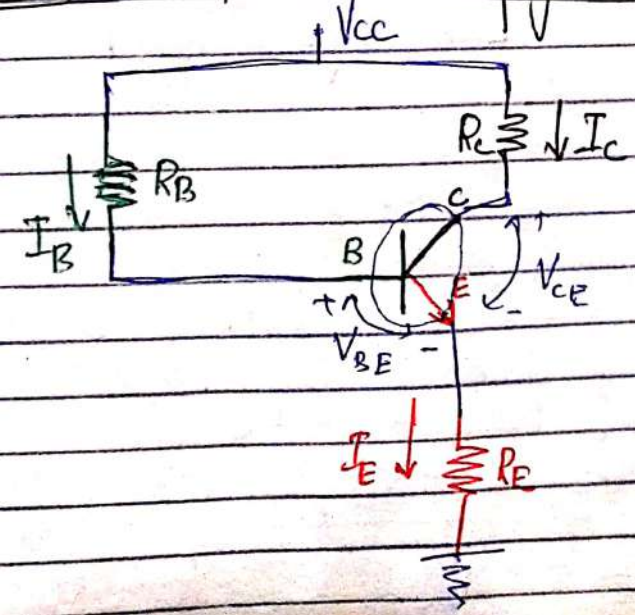
(d) KVL to i/p loop.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{17.96 - 0.7}{20\mu}$$

$$\Rightarrow R_B = 862.3\ k\Omega$$

Emitter Bias Configuration.



We improve the stability of Q point by introducing emitter resistance R_E.

KVL to i/p loop

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

As $I_E = I_C + I_B$

and $I_C = \beta I_B$

$$\Rightarrow I_E = (\beta + 1) I_B$$

$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$$

$$V_{CC} - I_B [R_B + (\beta+1) R_E] - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E}$$

As $I_C = \beta I_B$

$$\Rightarrow \boxed{I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E} \right]}$$

For V_{CE};

KVL to o/p loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

As $I_E \approx I_C$

$$\Rightarrow V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$\Rightarrow \boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

Advantage of using R_E

Once Q point is fixed, we don't want it to change.

If I_C changes ⇒ Q point will also change

I_C changes b/c of two things.

① temperature

If T ↑ ⇒ I_C ↑

As $I_C = \beta I_B + (\beta+1) I_{CBO}$

How R_E saves from increased I_C? temp

I_C ↑ ⇒ $I_E R_E$ ↑ (As $I_C \approx I_E$) ⇒ I_B ↓

As i/p KVL eq ⇒ ⇒ I_C ↓

$$I_B = \frac{V_{CC} - V_{BE} - I_E R_E}{R_B}$$

② β value

changes I_C as $I_C = \beta I_B$

As $$I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E} \right]$$

$\beta+1 \approx \beta$

$$I_C = \beta \left(\frac{V_{CC} - V_{BE}}{R_B + \beta R_E} \right)$$

$\beta R_E >> R_B$ neglecting R_B

β cancels out.

$$I_C = \frac{V_{CC} - V_{BE}}{R_E}$$ so indepent of β.

Disadvantage of Using R_E:

Inorder to make I_C independent of β, the condition must be met is;

$$\beta R_E >> R_B$$

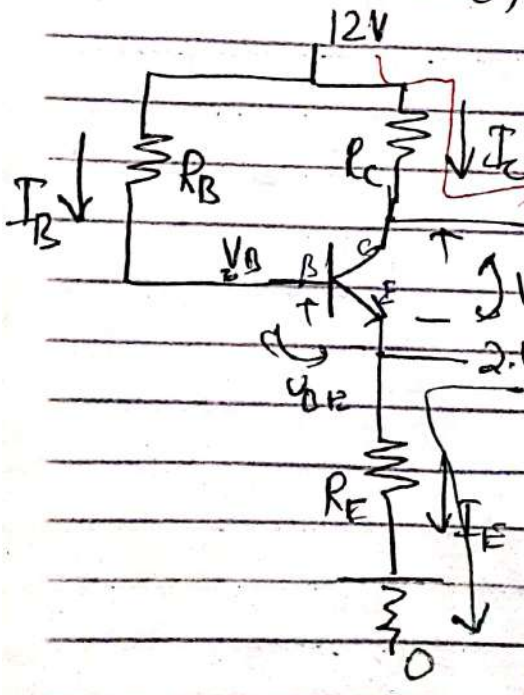
but mostly β is unknown to us.

So to achieve this condition

(i) $R_E \uparrow\uparrow \Rightarrow V_{CC} \uparrow\uparrow$ ⇒ Increased cost and precautions.

(ii) $R_B \downarrow\downarrow$ ⇒ Reverse bias of collector base junction will reduce.

Q. For the emitter bias configuration; determine R_C, R_E, R_B, V_{CE} & V_B.



Given $\beta = 80$

$I_C = 3mA$ $V_C = 7.6V$

$V_E = 2.4V$ $V_{CC} = 12V$

Solution.

(c) V_B

$V_{BE} = 0.7V$ → forward biased silicon diode

$V_B - V_E = 0.7$

$V_B = 0.7 + 2.4 \Rightarrow V_B = 3.1\,V$

(d) V_{CE} (o/p voltage).

$V_{CE} = V_C - V_E = 7.6 - 2.4$

$\Rightarrow V_{CE} = 5.2\,V$

(c) R_B

KVL to I/P loop $+12 - I_B R_B = 3.1V$

$I_B = \frac{I_C}{\beta} = \frac{3m}{80} \Rightarrow I_B = 37.5\mu A$

$\Rightarrow R_B = \frac{12 - 3.1}{37.5\mu} \Rightarrow R_B = 237\,K\Omega$

(b) R_E

KVL as indicated.

$2.4 - I_E R_E = 0$

$I_E \approx I_C = 3mA$

$R_E = \frac{2.4}{3m} \Rightarrow R_E = 0.8\,K\Omega$

(a) R_C

KVL as indicated

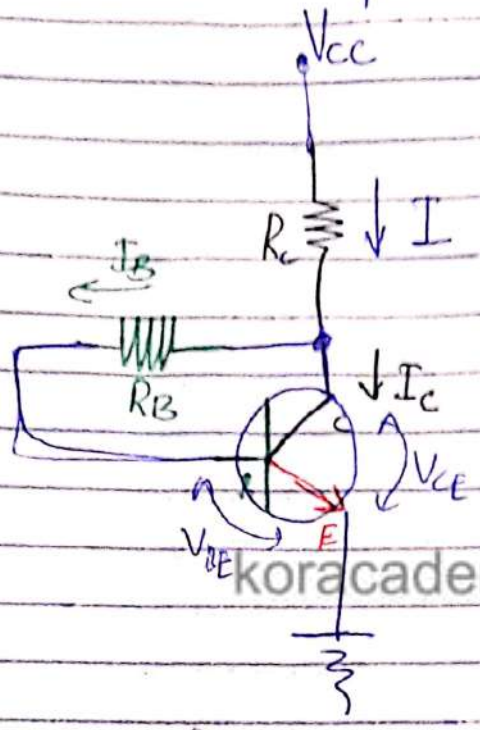
$12 - I_C R_C = 7.6$

$R_C = \frac{12 - 7.6}{3mA} \Rightarrow R_C = 1.47\,K\Omega$

Collector Feedback Biasing

Introducing feedback from collector to base

First we will calculate I_C and V_{CE} (these are coordinates of the Q point).



KCL at the node

$$I = I_B + I_C$$

For I_B

KVL to i/p loop

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

As $I_C = \beta I_B$

$$\Rightarrow V_{CC} - [(\beta+1)R_C + R_B] I_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_C}$$

As $I_C = \beta I_B$

$$\Rightarrow \boxed{I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_C} \right]}$$

y coordinate of Q pt

For V_{CE} KVL to o/p loop.

$$V_{CC} - IR_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_B + I_C) R_C$$

Advantages

stabilizes Q point (i) against the variation of temperature.

(ii) against variation of biasing voltage.

(iii) " " " of β value.

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + (\beta + 1) R_C}$$

$\beta + 1 \approx \beta$

$\beta R_C > R_B$

so neglecting R_B.

β cancels out.

$$\Rightarrow I_C = \frac{V_{CC} - V_{BE}}{R_C}$$

Disadvantages

$\beta R_C >> R_B$

Mostly β is unknown.

so $R_C \uparrow\uparrow \Rightarrow I_C \uparrow$ is squared.

or

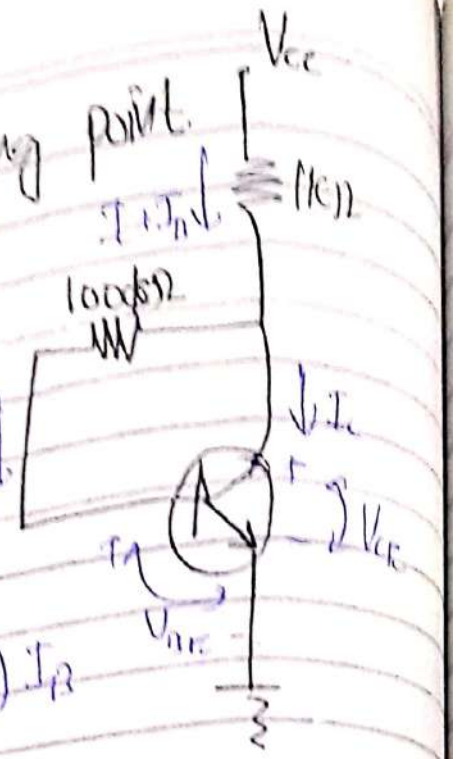
$R_B \downarrow\downarrow \Rightarrow$ R.B of collector base junction will reduce.

Q. Determine the operating point.

$V_{cc} = 20V$ $R_c = 1K\Omega$

$R_B = 100K\Omega$ $\beta = 100$

Q point (V_{CE}, I_C)



KVL to I/P loop

$V_{cc} - (I_c + I_B)(1K) - (100k) I_B - V_{BE} = 0$

$V_{BE} = 0.7$ (silicon)

$I_c = \beta I_B$

$I_B = \frac{V_{cc} - 0.7}{(\beta + 1)(1K\Omega) + 100K\Omega}$

$= \frac{20 - 0.7}{(100+1) R_c + R_B}$ $\Rightarrow I_B = 0.096\ mA$

$\Rightarrow I_B = 96\mu A$.

$I_c = \beta I_B = (100)(96\mu A)$

$\Rightarrow \boxed{I_c = 9.6\ mA}$

For V_{CE}:

KVL to O/P loop

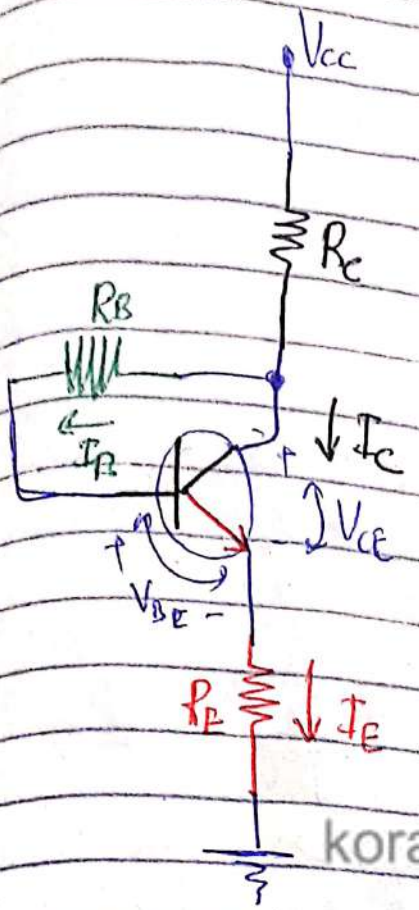
$20 - (I_c + I_B)(1K\Omega) - V_{CE} = 0$

$V_{CE} = 20 - (9.6m + 0.096m)(1K)$

$\Rightarrow V_{CE} = 10.304\ V$

$\Rightarrow$ Q point = $(10.304V, 9.6mA)$

Collector Feedback Biasing With Emitter Resistance



For I_B

KVL to i/p loop

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

As $I_E = I_C + I_B$

$I_C = \beta I_B$

$\Rightarrow I_E = (\beta+1) I_B$

$$\Rightarrow V_{CC} - (\beta+1) I_B R_C - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$$

$$\Rightarrow V_{CC} - I_B[(\beta+1)(R_C+R_E) + R_B] - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)(R_C+R_E)}$$

$- I_C = \beta I_B.$

$$I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_B + (\beta+1)(R_C+R_E)} \right]$$

If the anditon: $(\beta+1)(R_C+R_E) >> R_B$ is met, then I_C beames indepedent of β valve.

(as we ignre R_B and then β cancels out).

For V_{CE} KVL to o/p loop

$$V_{CC} - (I_C + I_{R2})R_C - V_{CE} - I_E R_E = 0$$

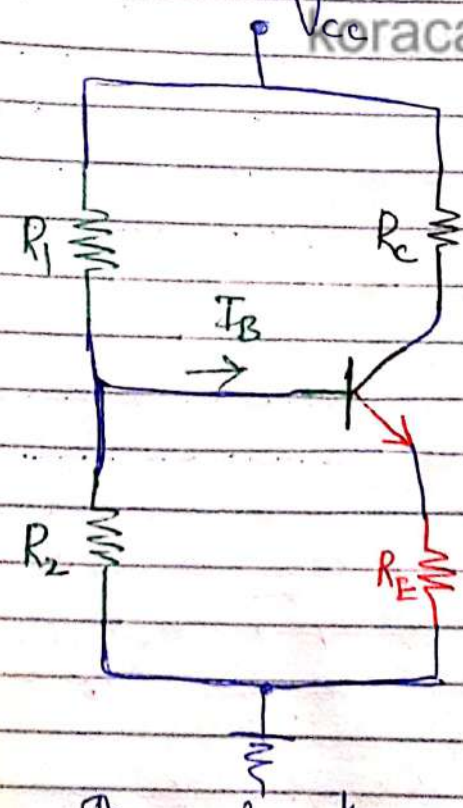
$$V_{CC} - I_E R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} - I_E(R_C + R_E) - V_{CE} = 0$$

$$I_E \approx I_C$$

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

Voltage Divider Bias configuration

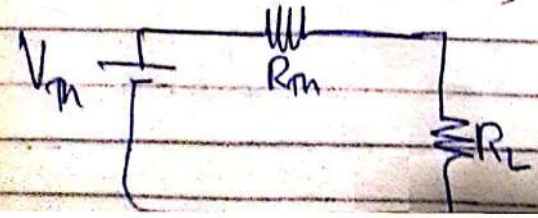


Called V.D.B because of the voltage divider network (combination of R_1 and R_2) is used to bias the transistor.

No resistance R_B.
↳ Instead of it we have two resistors R_1 and R_2.

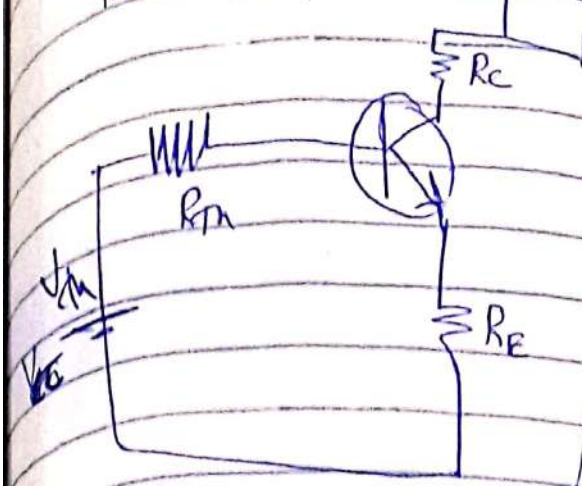
We need to find the operating point.

Thevenin's theorem;

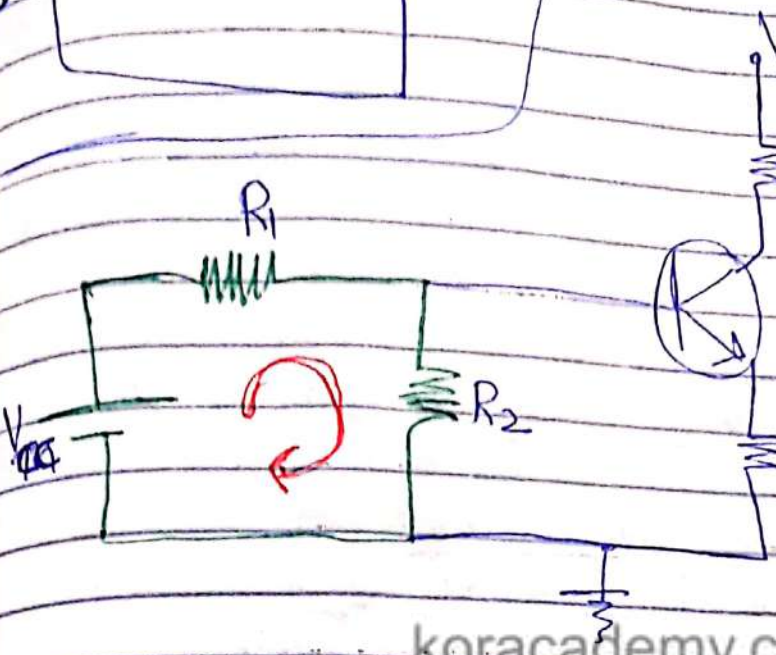


(load is the right side)

The thevenin equivalent model would be as;

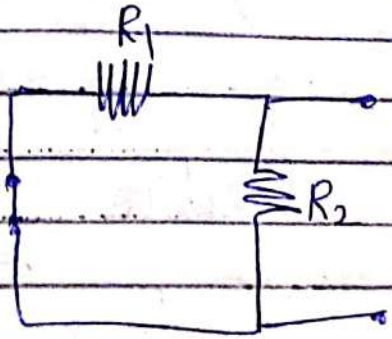


Using potential difference instead of potential at point.



Short crait the voltage source and open crait the load.

ie



$$R_{Th} = R_1 \,||\, R_2$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

Find current in the ~~load~~ loop and then voltage across the load (or R_2).

KVL

$$I = \frac{V_{cc}}{R_1 + R_2}$$

$$V_{Th} = IR_2 \Rightarrow V_{Th} = \frac{R_2 V_{cc}}{R_1 + R_2}$$

Similar to emitter bias configuration.

In place of R_B we have R_{Th}.
In place of V_{cc} we have V_{Th}.

To find I_C we calculate I_B first.

KVL to i/p loop

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

As $I_E = (\beta+1) I_B$

$$V_{Th} - I_B R_{Th} - V_{BE} - (\beta+1) I_B R_E = 0$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1) R_E}$$

As $I_C = \beta I_B$

$$\Rightarrow \boxed{I_C = \beta \left[\frac{V_{Th} - V_{BE}}{R_{Th} - (\beta+1) R_E} \right]}$$

For I_C to be independent of β.

$(\beta+1) R_E >> R_{Th}$

↳ ignored → β cancels out.

V_{CE}. KVL to o/p loop

$$V_{cc} - I_C R_C - V_{CE} - I_E R_E = 0$$

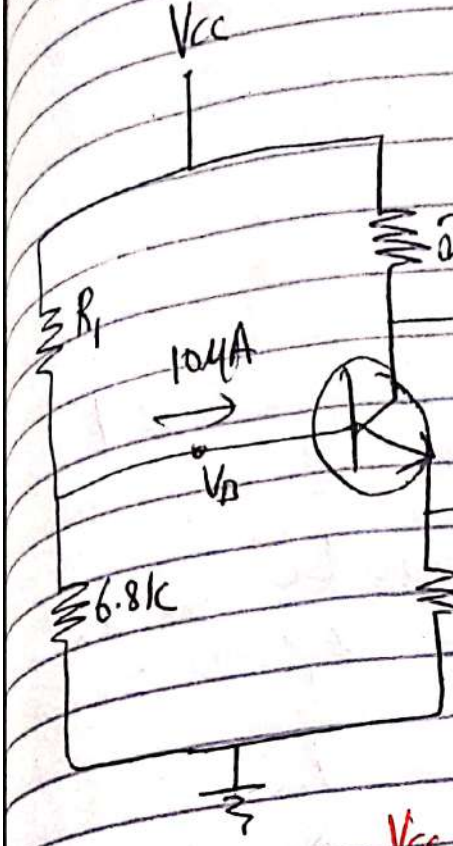
$I_E \approx I_C$

$$V_{cc} - I_C (R_C + R_E) - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Q: For the following configuration, determine: I_C, V_E, V_{CC}, V_{CE}, V_B, R_1.

Given $I_B = 20\mu A$ $R_C = 2.7k\Omega$
$R_E = 1.2k\Omega$ $V_C = 10.6V$
$\beta = 100$ $R_2 = 6.8k\Omega$

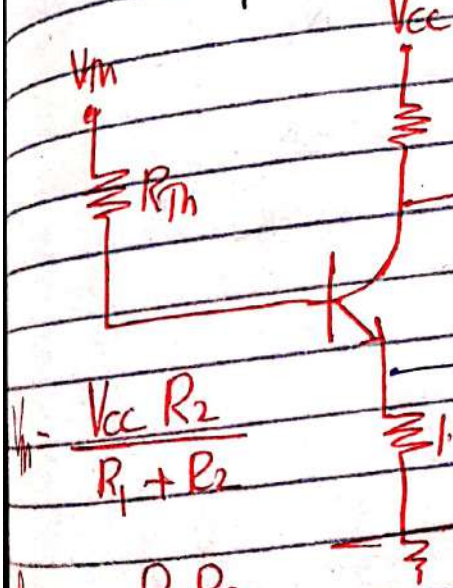


Solution

(a) I_C

$I_C = \beta I_B$
$= (100)(20\mu)$
$\Rightarrow I_C = 2mA.$

Drawing the Thevenin eq ckt



(c) V_{CC}

$V_{CC} - I_C R_C = 10.6$
$V_C = 10.6 + (2m)(2k)$
$V_{CC} = 16V$

$V_{th} = \frac{V_{CC} R_2}{R_1 + R_2}$

$R_{th} = \frac{R_1 R_2}{R_1 + R_2}$

(b) V_E

$\because I_E = I_C + I_B$

$I_B \downarrow \Rightarrow I_E \approx I_C$

$I_E = 2mA + 0.02mA$
$= 2.02mA$

KVL $V_E - I_E R_E = 0$

$V_E = (2.02\,m)(1.2\,k)$

$\Rightarrow V_E = 2.4\,V$

(d) V_{CE}

$V_{CE} = V_C - V_E = 10.6 - 2.4$

$\Rightarrow V_{CE} = 8.17\,V$

(e) V_B

$V_{BE} = V_B - V_E$

$0.7 = V_B - 2.4 \Rightarrow V_B = 3.12\,V$

(f) R_1

base current is very small so the drop across R_{Th} is also very small.

$V_{Th} \approx V_B$ actually potential at ↵ point

$V_{Th} = \frac{V_{CC} R_2}{R_1 + R_2}$

$3.124 = \frac{(16)(6.8k)}{R_1 + 6.8k}$

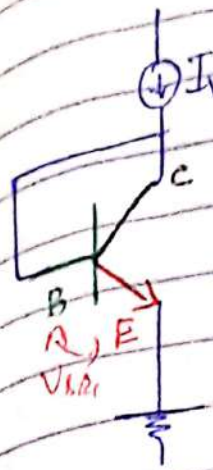
$\Rightarrow R_1 = 28k\Omega$

Current Mirror Circuit

The circuit which is forced to output current equal to input current.
ie output current should be mirror image of input current.

I_{in} → [C.M.C] → $I_{out} = I_{in}$

or I_{source} or $I_{sink} = I_{source}$



Collector base junction is shorted

$V_{CB} = V_C - V_B$

As $V_C = V_B$

$\Rightarrow V_{CB} = 0V$.

→ Diode connected transistor.

β = large = α

$I_B = 0A$ $\quad I_C = I_E$

The current equation of a diode in forward bias is,

$$I_E = I_0 e^{V_{BE}/V_T}$$

where

I_0 → Reverse saturation current V_T → Thermal voltage

$$V_T = \frac{T}{11600} \quad (T \text{ in } ^\circ K)$$

$I_E = I_C = I_{ref}$

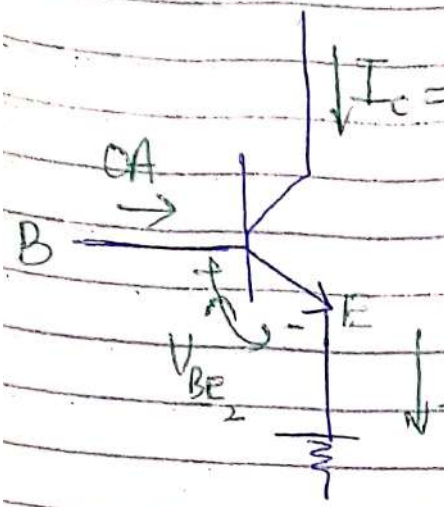
$$I_{ref} = I_0 e^{V_{BE1}/V_T}$$

$$\frac{I_{ref}}{I_0} = e^{V_{BE1}/V_T}$$

$$\ln\left(\frac{I_{ref}}{I_0}\right) = \ln\left(e^{V_{BE1}/V_T}\right)$$

$$V_{BE1} = V_T \ln\left(\frac{I_{ref}}{I_0}\right) \rightarrow (1)$$

let a normal npn transistor.



$I_c = I_E = I_{out} = I_0 e^{V_{BE}/V_T}$

$V_{BE_2} = V_T \ln\left(\frac{I_{out}}{I_0}\right) \rightarrow (1)$

If $V_{BE_1} = V_{BE_2}$

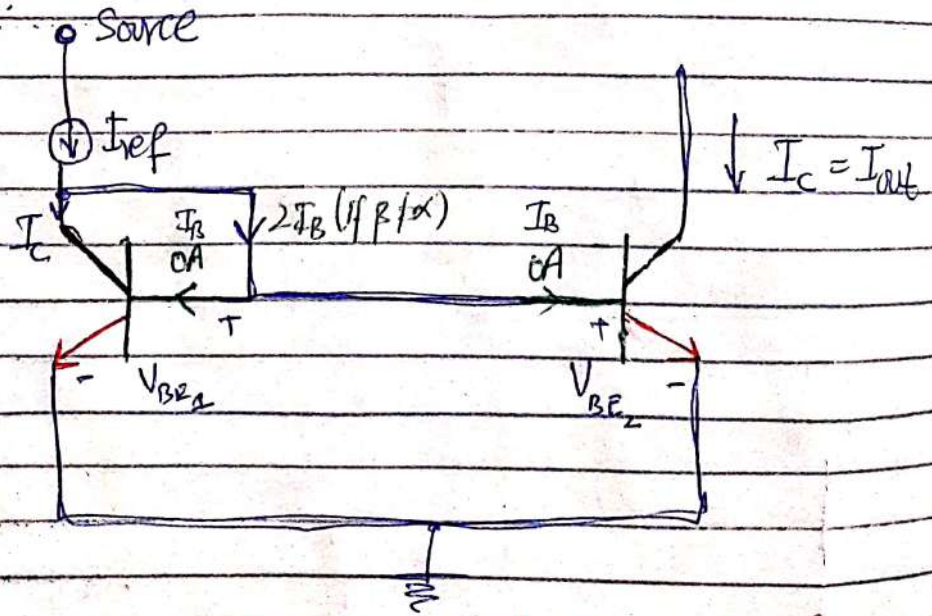
$\Rightarrow V_T \ln\left(\frac{I_{ref}}{I_0}\right) = V_T \ln\left(\frac{I_{out}}{I_0}\right)$

$\ln\left(\frac{I_{ref}}{I_0}\right) = \ln\left(\frac{I_{out}}{I_0}\right)$

$I_{out} = I_{ref}$

Arrangement?

To make both base to emitter voltages same.



Basic current mirror circuit.

If $\beta \neq \alpha \Rightarrow I_B \neq 0$

$$I_{ref} = I_C + 2I_B$$

$$I_{ref} = I_C + 2\left(\frac{I_C}{\beta}\right)$$

$$I_{ref} = I_C\left(\frac{\beta+2}{\beta}\right)$$

As $I_C = I_{out}$

$$\Rightarrow I_{ref} = I_{out}\left(\frac{\beta+2}{\beta}\right)$$

or $$\boxed{I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}}$$

Requirement of current mirror circuit?

(i) Both transistors should be in active region.

(ii) Both transistors should be identical and perfectly matched.

→ $V_{BE_1} = V_{BE_2} = V_{BE}$ $I_{C1} = I_{C2} = I_C$

$I_{B1} = I_{B2} = I_B$ $\beta_1 = \beta_2 =$ large

(iii) Junction area of emitter should be identical for both transistors

$$A_{E1} = A_{E2}$$

$A_E \propto I_o$

let $A_{E_2} = 2A_{E_1}$

$$I_{O2} = 2 I_{O1}$$

$$V_{BE_2} = V_T \ln \frac{I_{out}}{I_{O2}}$$

$\beta = \alpha$

$$V_{BE_1} = V_T \ln \frac{I_{ref}}{I_{O1}}$$

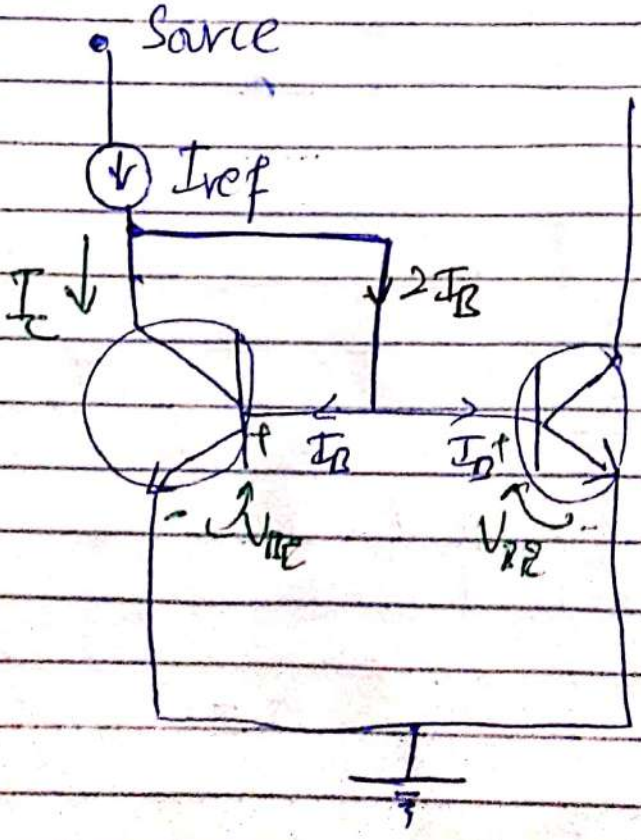
$$V_{BE_1} = V_{BE_2} \Rightarrow \frac{I_{out}}{I_{O2}} = \frac{I_{ref}}{I_{O1}}$$

$$\frac{I_{out}}{2 I_{O1}} = \frac{I_{ref}}{I_{O1}}$$

$$I_{out} = 2 I_{ref}$$

(If the area is greater, current will be greater in the same proportion).

① The basics of current mirror is as;

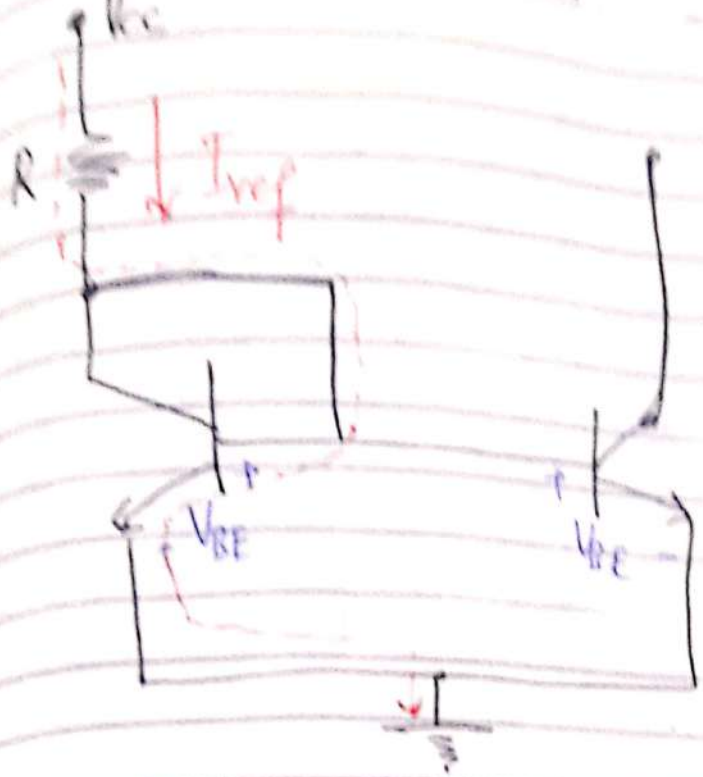


$I_{out} = I_{ref}$ ($\beta = \alpha$)

$$I_{out} = \left(\frac{\beta}{\beta + 2}\right) I_{ref}$$

If ($\beta \neq \alpha$) I_{out} very less

A prestim can be framed as,



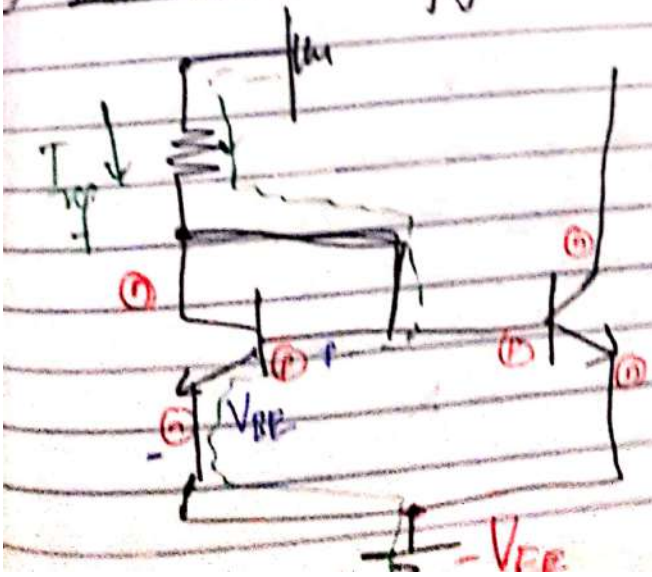
To find Iref, apply KVL as shown.

$V_{cc} - I_{ref}(R) - V_{BE} = 0$

$$I_{ref} = \frac{V_{cc} - V_{BE}}{R}$$

p connected to positive
n connected to ground.

Let another figure.



This is an ideal circuit unless the ground is replaced by $-V_{EE}$.

n → -ve
p → ground.

If Vee is ve again ideal.

For I_{ref} → apply KVL as shown

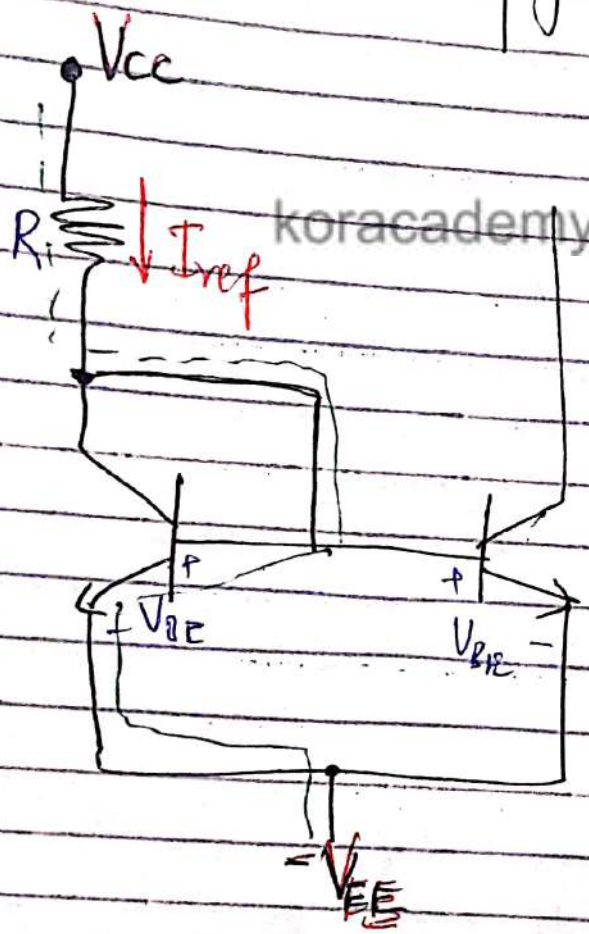
$$0 - I_{ref}(R) - V_{BE} = 0 - V_{EE}$$

$$I_{ref} = \frac{V_{EE} - V_{BE}}{R}$$

$I_{out} = I_{ref}$ $(\beta = \alpha)$

$I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}$ (if β is finite large value)

④ Another valid configuration of a C-M-C



$$I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}$$

(or)

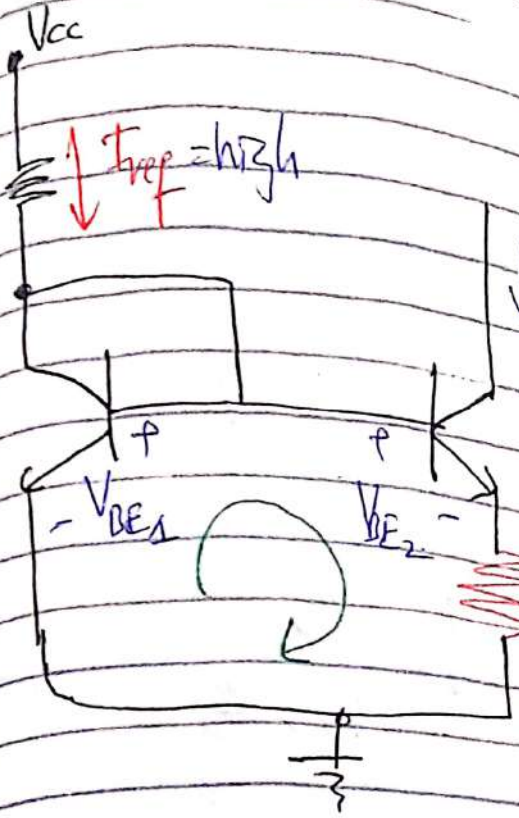
$$I_{out} = I_{ref} \quad (\beta < \alpha)$$

To calculate I_{ref}, apply KVL.

$$V_{cc} - I_{ref}(R) + 0 - V_{BE} = -V_{EE}$$

$$I_{ref} = \frac{V_{cc} + V_{EE} - V_{BE}}{R}$$

Widlar Current Mirror Circuit



$V_{BE_1} \neq V_{BE_2}$

$I_{out} \neq I_{ref}$

$I_{out} = low\ (\mu A)$

$I_{ref} = high\ (mA)$

Used for obtaining low o/p I from high i/p

Calculating R_E ?

$$V_{BE_1} = V_T \ln\left(\frac{I_{ref}}{I_o}\right)$$

$$V_{BE_2} = V_T \ln\left(\frac{I_{out}}{I_o}\right)$$

Apply KVL to the loop.

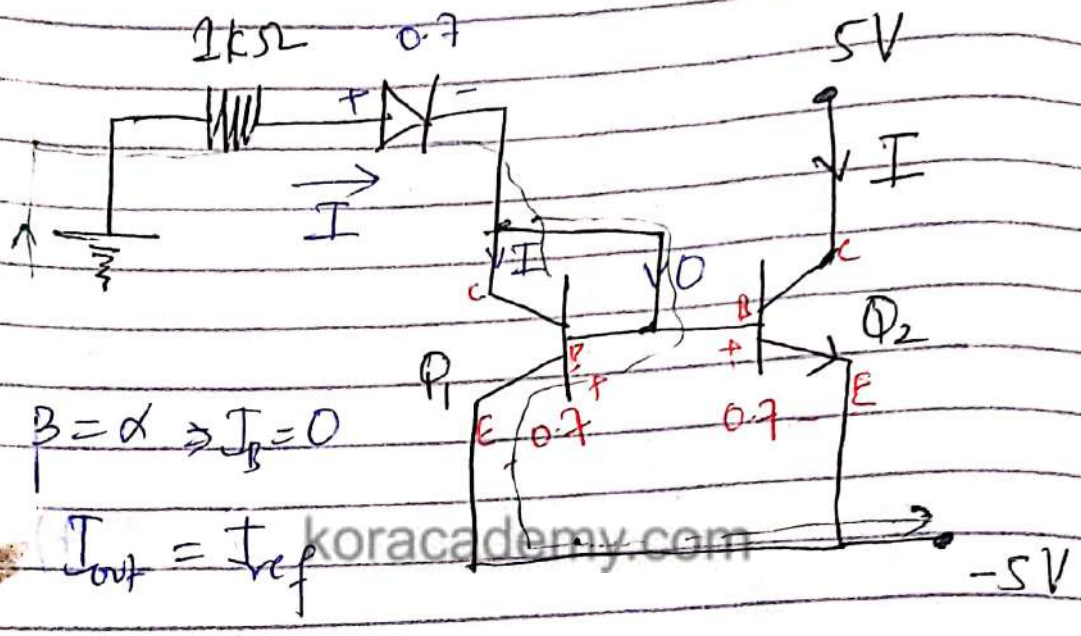
$$V_{BE_1} - V_{BE_2} - I_{out}(R_E) = 0$$

$$I_{out}(R_E) = V_{BE_1} - V_{BE_2} \quad \because \ln(x-y) = \ln\left(\frac{x}{y}\right)$$

$$I_{out}(R_E) = V_T \ln\left(\frac{I_{ref}}{I_o}\right)$$

$$R_E = \frac{V_T}{I_{out}} \ln\left[\frac{I_{ref}}{I_{out}}\right]$$

Q. Two perfectly matched silicon transistors are connected as shown. Assuming β to be very high and the forward voltage drop in diodes to be 0.7V, I is -3.6mA.



$\beta = \alpha \Rightarrow I_B = 0$

$I_{out} = I_{ref}$

transistors and diode is forward biased.

Apply KVL

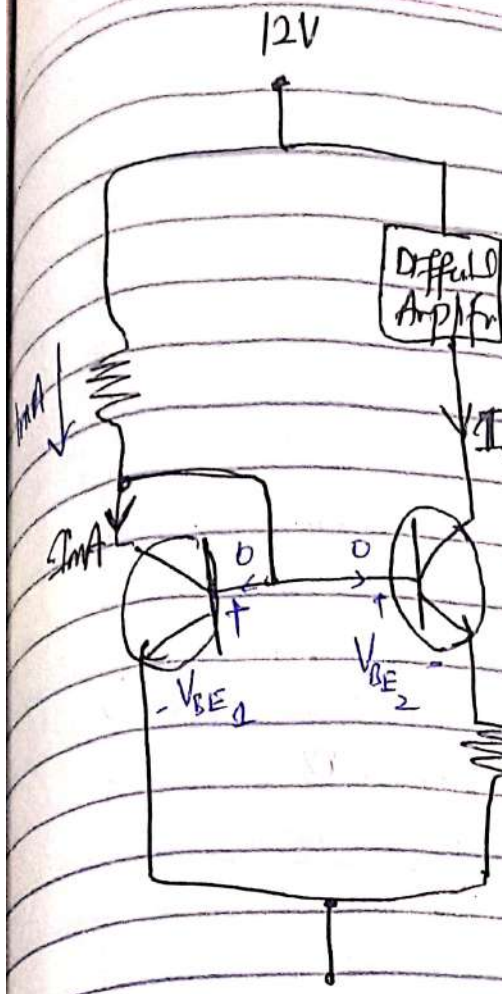
$$I_C(I) - 0.7 - 0.7 = -5$$

$$I = -3.6 \text{ mA}$$

(V, mA, kΩ)

Q. Perfectly matched transistors with $V_T = 25$mV. $I_B \approx 0$.
The value of resistance R in kΩ that is required to provide 1μA bias current for the differential amplifier stack is

172 kΩ.



$V_T = 25mV$

$I_B = 0.4A$ & $\beta = \alpha$

$I_{out} = 1\mu A$ $R = ?$

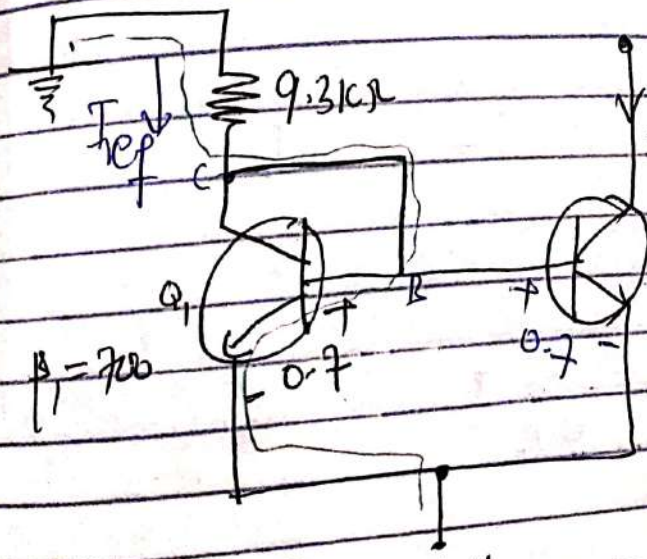
This figure is of widler current mirror circuit.

$$R_E = \frac{V_T \ln\left[\frac{I_{ref}}{I_{out}}\right]}{I_{out}}$$

$$R = R_E = \frac{25\times10^{-3}}{1\times10^{-6}} \ln\left[\frac{1\times10^{-3}}{1\times10^{-6}}\right]$$

$$\Rightarrow \boxed{R = 172.7\ K\Omega}$$

Q. In the silicon BJT circuit shown, assume that the emitter area of transistor Q_1 is half that of that of transistor Q_2. The value of I_o is 2mA.



$$A_{E_1} = \frac{A_{E_2}}{2}$$

or

$$A_{E_2} = 2A_{E_1}$$

$$I_{E_2} = 2I_{E_1}$$

$$I_{C_2} = 2I_{C_1}$$

$$\Rightarrow I_o = 2I_{ref}$$

High value of β so base current neglegible.

Apply KVL

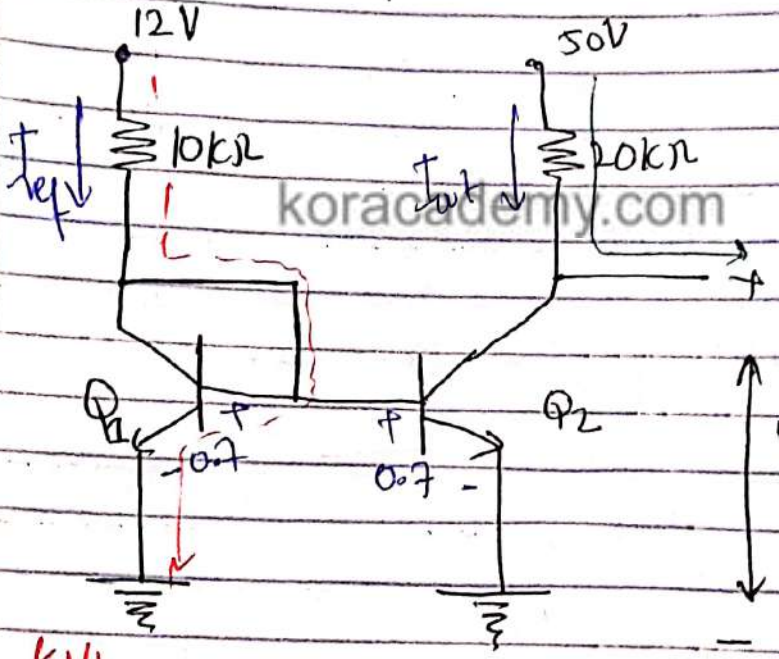
$0 - I_{ref}(9.3k) - 0.7 = -10$

$\Rightarrow I_{ref} = 1\,mA$

$I_o = 2 I_{ref} = 2(1mA)$

$\Rightarrow I_o = 2\,mA$

Q. The matched transistors Q_1 and Q_2 shown have $\beta = 100$. Assuming the base emitter voltages to be 0.7 V, the collector emitter voltage V_2 of transistor Q_2 is 28 V.



$I_{out} = \left(\frac{\beta}{\beta+2}\right) I_{ref}$

KVL

$50 - 20k(I_o) = V_2$

$V_2 = 50 - 20k(I_o)$ ↳ (A)

$I_{ref} = ?$

KVL

$12 - 10k(I_{ref}) - 0.7 = 0$

$I_{ref} = \frac{12 - 0.7}{10k} \Rightarrow I_{ref} = 1.13\,mA$

$I_{out} = \left(\frac{100}{102}\right)(1.13\,mA)$

(A) $\Rightarrow V_2 = 27.84$ Volt

BJT AC Analysis

→ Examine the AC response of transistors. (we will use different transistor models)

In AC analysis first we need to decide whether to use small signal or large signal technique.

large signal amplifiers → power amplifiers

If we use large signal → I_B will increase

and $I_C = \beta I_B$

If $I_B \uparrow \Rightarrow I_C \uparrow \Rightarrow$ Q point will change

↳ this condition occurs in large signal analysis.

In S.S.A V_s is small and I_B will not change much.

Small signal can be defined as the signal having magnitude sufficiently small to keep the transistor in active region.

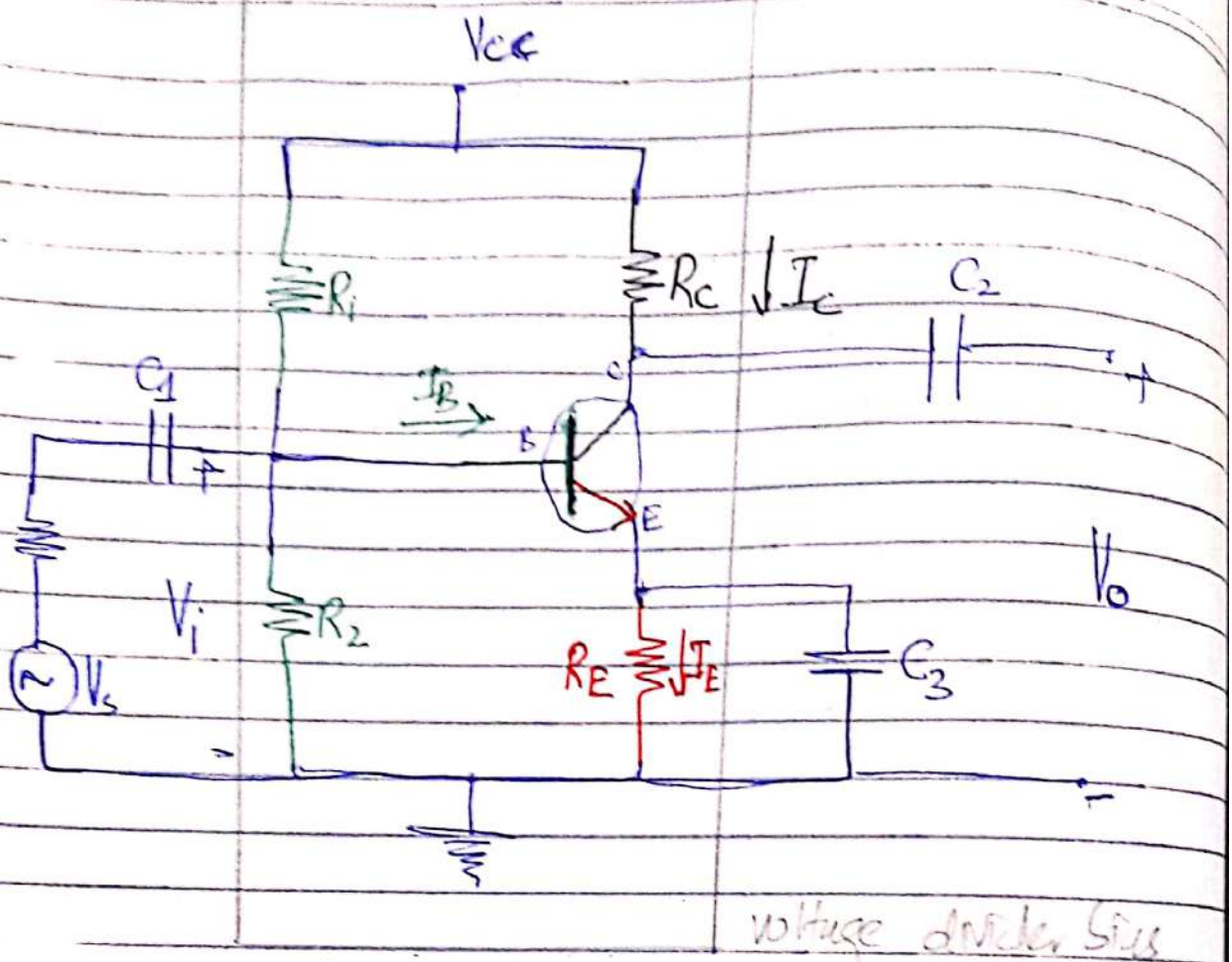
active region → because we want to use the transistor as amplifier.

C-B junction is reverse biased

E-B junction is forward biased.

Total response = dc response + ac response

For ac response we need to study the following (BJT amplifier) circuit.



voltage divider bias

In dc analysis ⇒ capacitors act as open circuit for dc signal.

In ac analysis → all the capacitors will act as short circuit for the AC signal.

Why?

C_1 and C_2 → coupling capacitors

C_3 → bypass capacitor

All the three capacitors have very high values of capacitance and because of this they behave as SC for ac signals.

$$X_C = \frac{1}{2\pi f C}$$

for dc $f = 0 \Rightarrow X_C = \infty \Rightarrow$ open circuit

for ac $f \neq 0$ C = large $X_C = \frac{1}{\text{large}}$

$\Rightarrow X_C \approx 0 \Rightarrow$ short circuit.

Coupling and Bypass?

C_1 and C_2 are called coupling capacitors b/c C_1 is coupling previous stage with the (V.d.b) circuit and C_2 is coupling the next stage with the (V.d.1) circuit.

We do not want the dc voltage from the previous or next stage to interfere with the dc biasing voltage (V_{cc}) because this will change the operating point.

$dc \rightarrow C \rightarrow \infty$

$C_3 \rightarrow$ bypass b/c it bypasses the AC signal.

The AC signal will have two different paths.

① through R_E ② through C_3

$C_3 \rightarrow$ zero reactance $\rightarrow$ AC signal. and hence R_E is short circuited b/c of C_3 in case of AC signal

Why short circuit R_E?

Gain reduces b/c of R_E.

If S.C $\Rightarrow$ gain will increase.

To find the AC response, we need do:

(i) Find the ac equivalent circuit.

(ii) Replace the transistor with its equivalent model.

AC Equivalent Circuit of BJT Amplifier

We have to simplify the circuit through the following three steps.

Step (i) Short circuit all the dc sources.

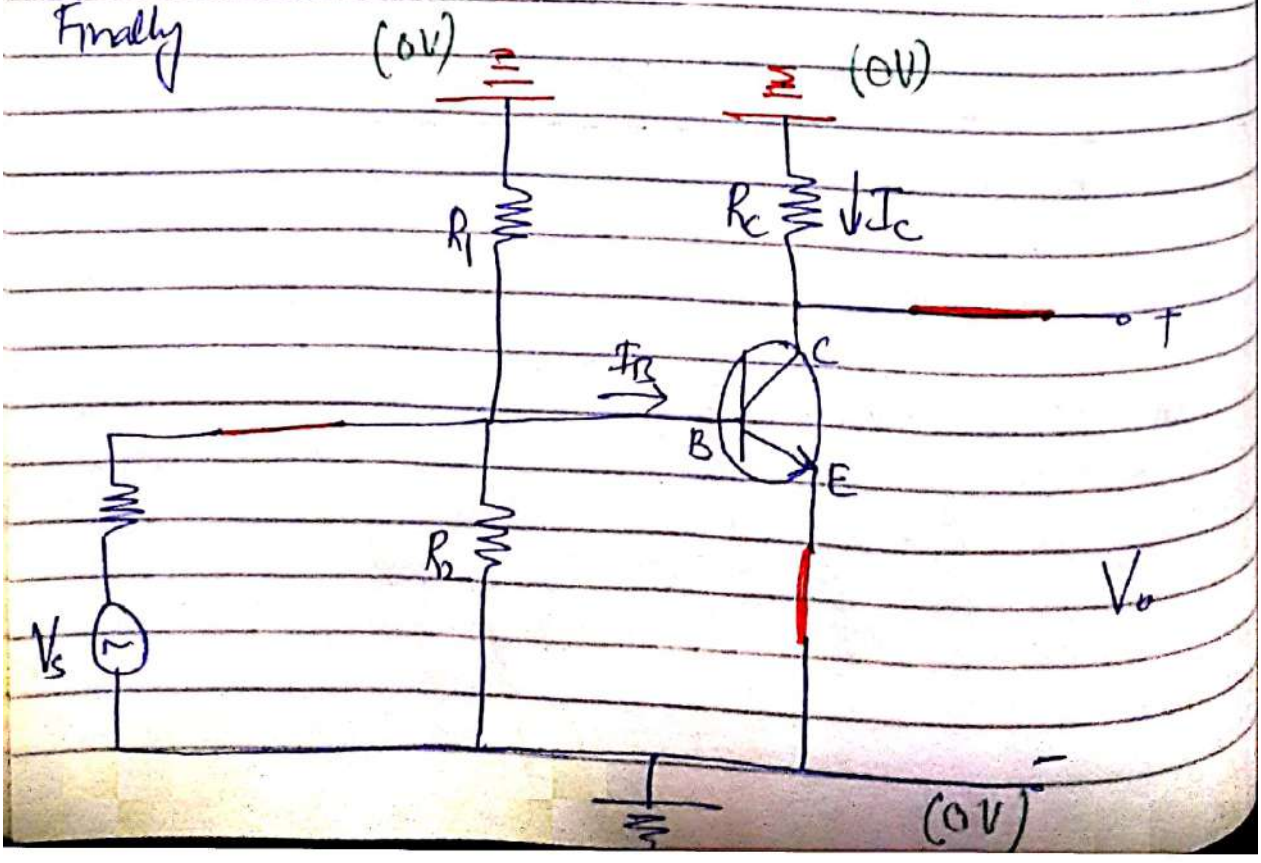
only V_{cc} → shorted → we have ground in its place.

Step 2 Short all the capacitors. C_1, C_2, C_3.

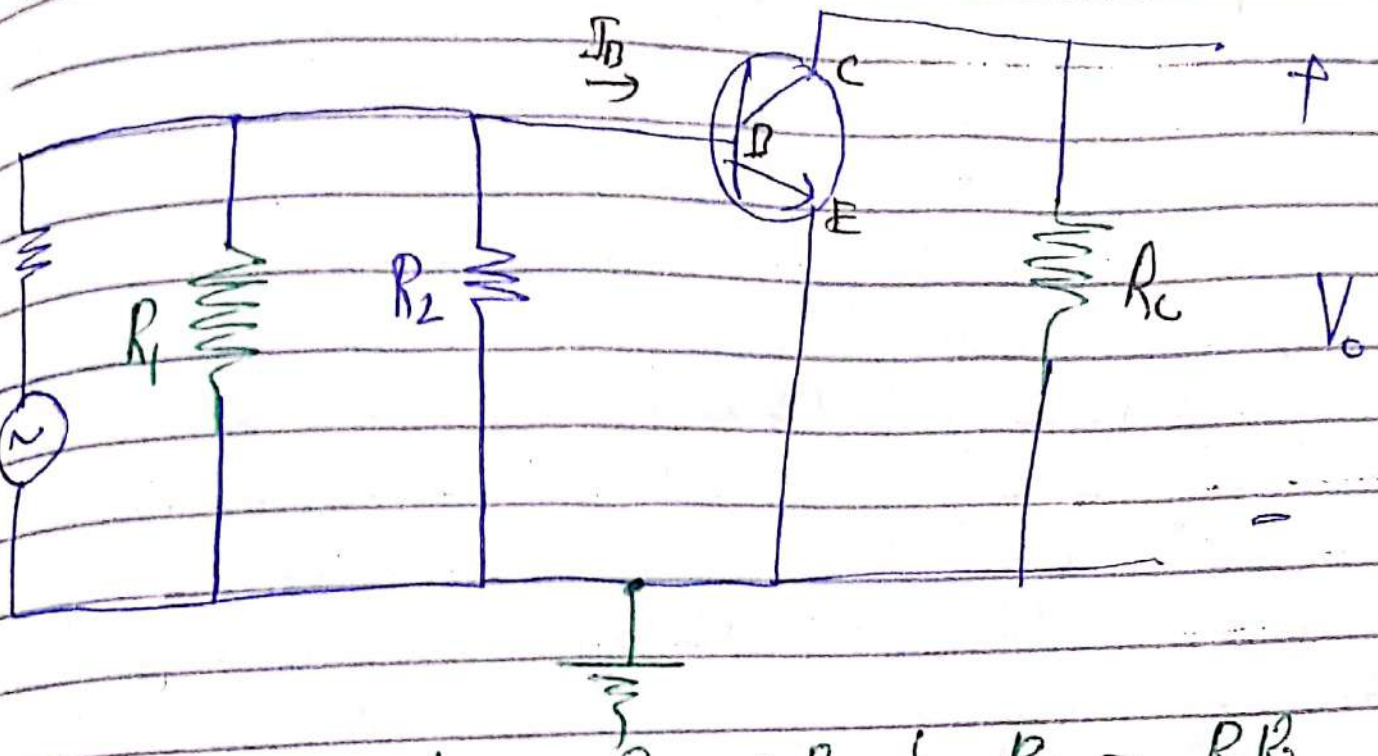
X_C $C \uparrow \Rightarrow X_C \approx 0$

Step 3 Redraw the network removing all the elements which are short circuited in step 1 and 2.

Finally



Further



We can replace R_1 and R_2 by $R_{eq} = \frac{R_1 R_2}{R_1 + R_2}$

Equivalent model?

It is a combination of circuit elements properly chosen to best represent the actual behaviour of device under specific operating point.

Equivalent models of transistor?

(i) hybrid model

(ii) re model (dynamic emitter resistance model)

(iii) hybrid π model.

All these three models are for small signals.

Hybrid Model

(Calculation of h parameters)

→ Equivalent model of transistor.
→ widely used before the popularity of r_e model.
→ Parameters are defined in general terms for any operating conditions.

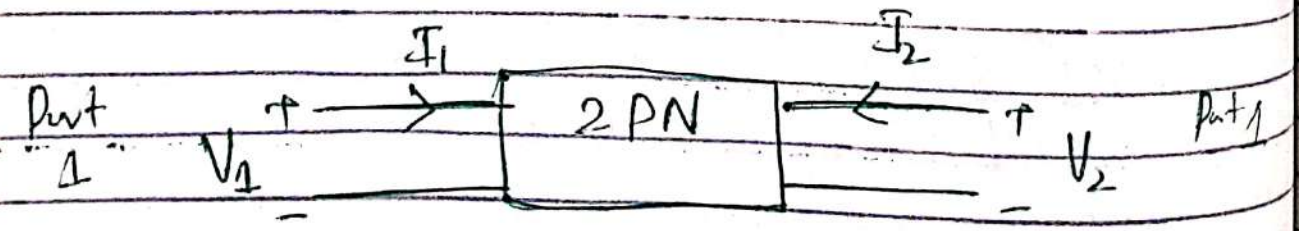
In r_e model, parameters are defined by the actual operating conditions.

We have to calculate h parameters and then draw the equivalent model.

Why hybrid?

Hybrid means mixed → and the parameters we will calculate have mixed dimensions.

A general two port network;



We are interested only in the terminal voltages and currents.

Transistor circuit is also a two port network.

I_1, V_1, I_2, V_2 are the total values ie the sum of their respective ac and dc values.

V_1 and I_2 ⇒ dependent

V_2 and I_1 ⇒ Independent

So we can say that;

$$V_1 = f_1(I_1, V_2)$$

$$I_2 = f_2(I_1, V_2)$$

$$\begin{pmatrix} V_1 \\ I_2 \end{pmatrix} = f \begin{pmatrix} I_1 \\ V_2 \end{pmatrix}$$

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \rightarrow (1)$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \rightarrow (2)$$

$h_i = h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0}$ dimensions of impedence when o/p is short circuited

$h_r = h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$ dimensionless reverse voltage gain when i/p is o.c

$h_f = h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$ dimensionless forward current gain when o.p is s.c

$h_o = h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$ dimensions of admittance o/p admittance with i/p o.c.

$$dV_1 = \frac{dV_1}{dI_1} dI_1 + \frac{dV_1}{dV_2} dV_2 \quad \rightarrow (1)$$

$$dI_2 = \frac{dI_2}{dI_1} dI_1 + \frac{dI_2}{dV_2} dV_2 \quad \rightarrow (2)$$

ac current = i ac voltage = v.

~~ac~~ ~~dc~~

changes will occur in ac and dc is fixed.

$$\Rightarrow \quad V_1 = h_{11} i_1 + h_{12} V_2$$
$$i_2 = h_{21} i_1 + h_{22} V_2$$

These equations are applicable to all three transistor configurations ie CB, CE, CC.

Nomenclature of h parameters

$h_{l_1 l_2}$

l_1 denotes the nature of parameter.
l_2 denotes the transistor configuration

eg I/P impedence of C.E is as h_{ie}

reverse voltage gain of C.B is as h_{rb}

O/p admittance of C.C is as h_{oc}

Forward current gain of C.B is as h_{fb}

Hybrid Equivalent Circuit

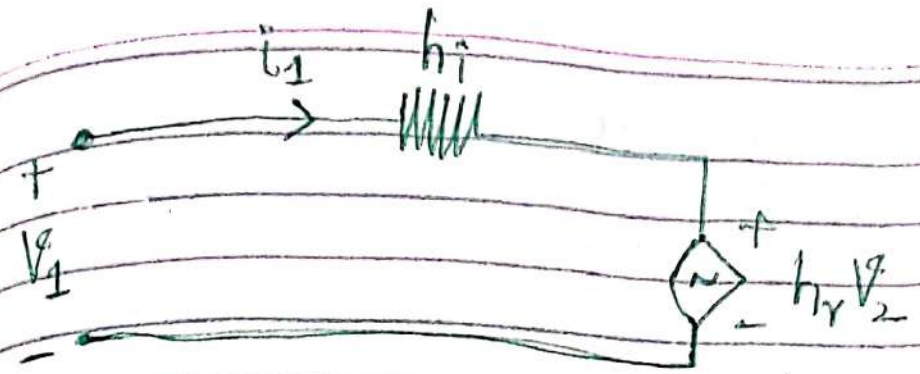
① $\leftarrow V_1 = h_i i_1 + h_r V_2$ (all units in volts)

② $\leftarrow i_2 = h_f i_1 + h_o V_2$ (all units in Amperes)

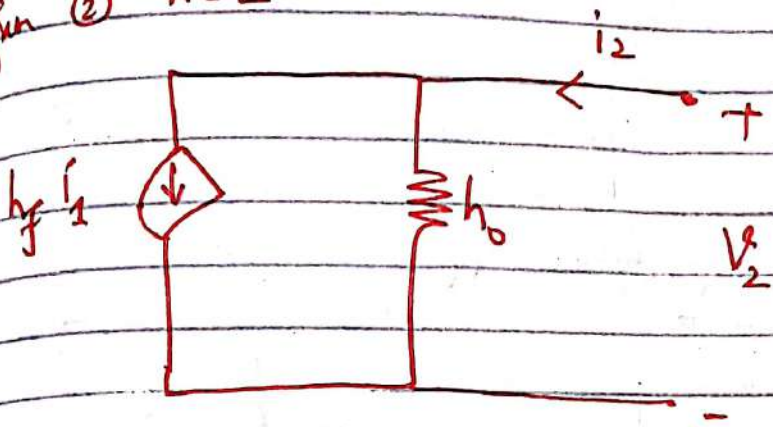
KVL $+V_1 - h_i i_1 - h_r V_2 = 0$

eq ckt:

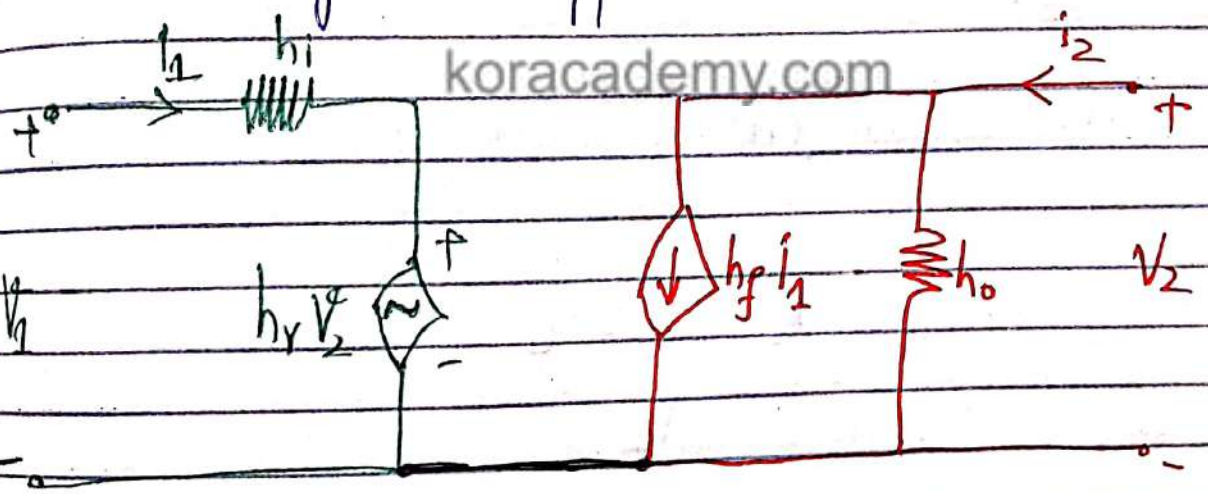
i_2 entering others leaving



for ② KCL



The final equivalent circuit is obtained by the combining the upper two.



In AC analysis the transistor is to be replaced by this eq model

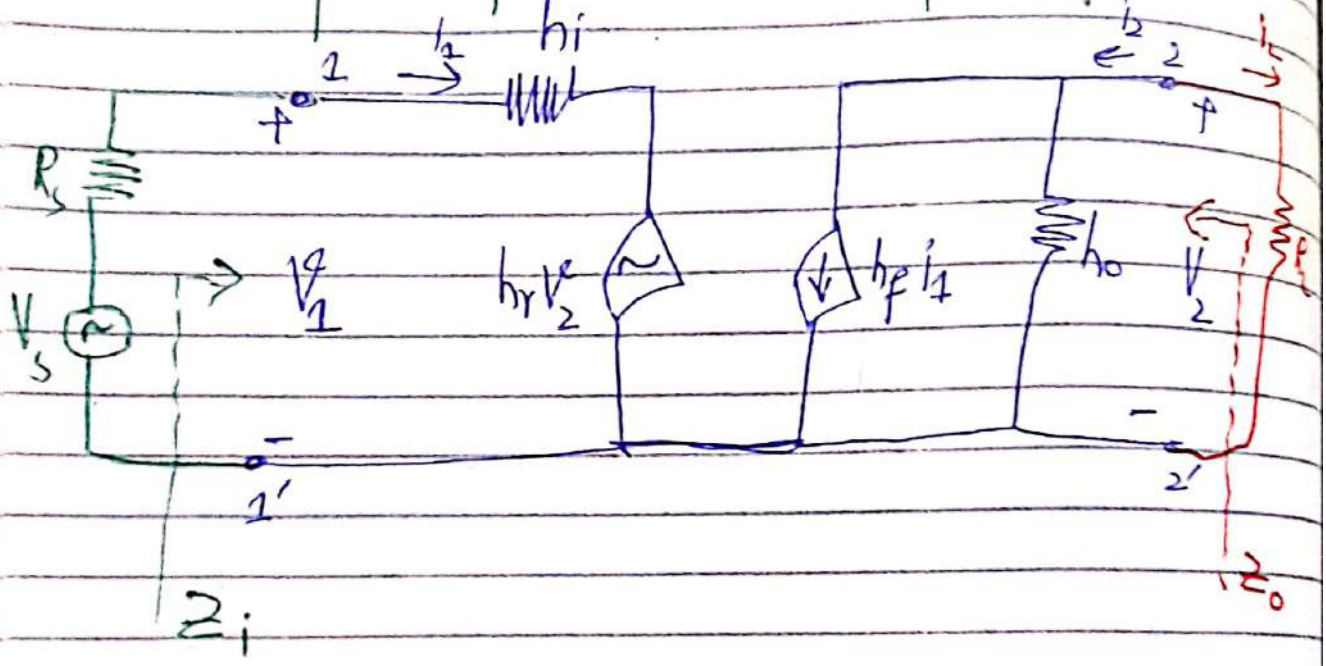
Analysis of Transistor Amplifier Using h parameters

We will find expressions for voltage, power and current gain

Introduce V_s and R_s to the i/p side and R_L to the o/p side.

$i_L \rightarrow$ current through R_L.

$Z_o \rightarrow$ o/p impedence $\quad Z_i \rightarrow$ i/p impedence



Current Gain (A_i) $\qquad A_i = \dfrac{\text{o/p } i}{\text{i/p } i} = \dfrac{i_L}{i_1}$

$$V_2 = i_L R_L = -i_2 R_L$$

As $\quad i_2 = h_f i_1 + h_o V_2$

$$\Rightarrow i_2 = h_f i_1 + h_o(-i_2 R_L)$$

or $\quad i_2 + h_o i_2 R_L = h_f i_1$

$$i_2(1 + h_o R_L) = h_f i_1$$

$$i_2 = \frac{h_f i_1}{1 + h_o R_L}$$

Putting in current gain.

$$A = \frac{-i_2}{i_1} = \frac{-h_f}{1 + h_o R_L}$$

The for CB, CE and CC.

Voltage Gain (A_V)

$$A_V = \frac{\text{o/p V}}{\text{i/p V}} = \frac{V_2}{V_1} = \frac{-i_2 R_L}{V_1}$$

$$A_i = \frac{-i_2}{i_1} \Rightarrow -i_2 = A_i i_1$$

$$A_V = \frac{i_1 A_i R_L}{V_1} = \frac{i_1 A_i R_L / i_1}{V_1 / i_1}$$

$$A_V = \frac{A_i R_L}{Z_i}$$

and $Z_i = h_i - \frac{h_r h_f}{\frac{1}{R_L} + h_o}$

$$A_i = \frac{-h_f}{1 + h_o R_L}$$

$$A_V = \frac{-h_f R_L}{h_i + (h_i h_o - h_r h_f) R_L}$$

Power Gain (A_P)

$$A_P = A_V \times A_i$$

$$= \left(\frac{-h_f R_L}{h_i + \Delta h R_L}\right)\left(\frac{-h_f}{1 + h_o R_L}\right)$$

$$A_P = \frac{h_f^2 R_L}{(h_i + \Delta h R_L)(1 + h_o R_L)}$$

Input Impedence (Z_i)

Impedence seen from terminals 1 and 1'

Ohms law $\Rightarrow V_i = i_1 \times Z_i$.

$$Z_i = \frac{V_1}{i_1} \qquad V_2 = -i_2 R_L$$

h parameter eq $V_1 = h_i i_1 + h_r V_2$

$$\Rightarrow V_1 = h_i i_1 + h_r (-i_2 R_L)$$

$$\frac{V_1}{i_1} = h_i - h_r \frac{i_2}{i_1} R_L$$

$$\frac{i_2}{i_1} = -A_i$$

$$\frac{V_1}{i_1} = h_i + h_r A_i R_L$$

$$Z_i = h_i + h_r \left(\frac{-h_f}{1 + h_o R_L} \right) R_L$$

$$\boxed{Z_i = h_i - \frac{h_r h_f}{1/R_L + h_o}}$$

Output Impedence (Z_o)

Impedence seen from terminals 2 and 2'

Two conditions to calculate Z_o;

(i) short circuit input source ie V_s. ($V_s = 0$)

(ii) open circuit output terminal. ($R_L = \infty$)

Ohms law $Z_o = \frac{V_2}{i_2}$

from h parameter eq $i_2 = h_f i_1 + h_o V_2$

$$Z_o = \frac{V_2}{h_f i_1 + h_o V_2} \rightarrow (1)$$

KVL to i/p loop

$$-i_1 R_s - i_1 h_i - h_r V_2 = 0$$

$$\Rightarrow i_1 (R_s + h_i) + h_r V_2 = 0$$

$$i_1 = \frac{-h_r V_2}{R_s + h_i}$$

Put i_1 in (1)

$$Z_o = \frac{V_2}{h_f \left(\frac{-h_r V_2}{R_s + h_i}\right) + h_o V_2}$$

$$\boxed{Z_o = \frac{R_s + h_i}{(h_o h_i - h_f h_r) + h_o R_s}}$$

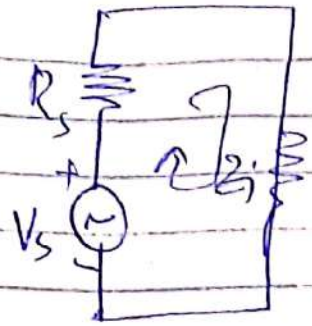
$$h_o h_i - h_f h_r = \Delta h$$

Overall Voltage Gain — (A_{VS})

The ratio of o/p voltage to the source voltage.

$$A_{VS} = \frac{V_2}{V_S} \times \frac{V_1}{V_1} = \frac{V_2}{V_1} \times \frac{V_1}{V_S}$$

$$A_{VS} = A_V \cdot \frac{V_1}{V_S}$$



$$V_s - iR_s - iZ_i = 0$$

$$i = \frac{V_s}{R_s + Z_i}$$

$$V_1 = iZ_i$$

$$V_1 = \frac{Z_i V_s}{R_s + Z_i} \Rightarrow \frac{V_1}{V_s} = \frac{Z_i}{R_s + Z_i}$$

$$\Rightarrow \boxed{A_{VS} = A_V \left(\frac{Z_i}{R_s + Z_i} \right)}$$

If V_s is ideal $\Rightarrow R_s = 0 \Rightarrow A_{VS} = A_V$

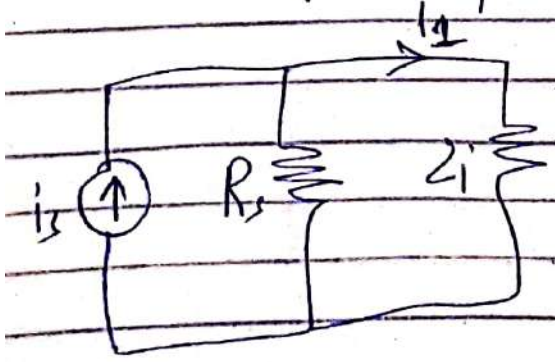
Overall Current Gain (A_{is})

Ratio of o/p current to the current delivered by the source.

$$A_{is} = \frac{i_L}{i_s} \times \frac{i_1}{i_1} = \frac{i_L}{i_1} \times \frac{i_1}{i_s} = \frac{-i_2}{i_1} \cdot \frac{i_1}{i_s}$$

$$A_{is} = A_i \cdot \frac{i_1}{i_s}$$

Finding i_1 / i_s



Using current divider rule.

$$i_1 = \frac{i_s R_s}{R_s + Z_i}$$

$$\Rightarrow \frac{i_1}{i_s} = \frac{R_s}{R_s + Z_i}$$

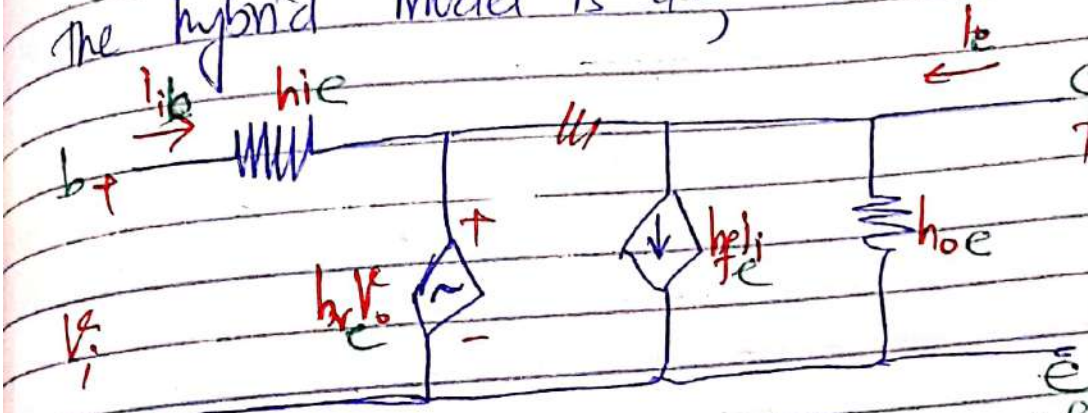
$$\Rightarrow \boxed{A_{is} = A_i \left(\frac{R_s}{R_s + z_i} \right)}$$

For ideal curent surce $R_s = \infty \Rightarrow A_{is} = A_i$

Approximate hybrid Equivalent model

Simplified form of hybrid model.

The hybrid model is as;



$I_i = I_b$ $I_o = I_c$ for CE configuration

For CE and CB; the magnitude of h_r and h_o are such that the results obtained for the parameters (eg z_i, z_o, A_v etc) are slightly effected if h_r and h_o are not included in this circuit.

→ Remove h_{re} and h_{oe}

h_o → o/p admittance $\frac{1}{h_o}$ → o/p impedance → very large

open cirt. ← neglect it

compare $\frac{1}{h_o}$ to R_L

$\frac{1}{h_o}$ very large

In fixed bias configuration we have R_C in parallel with R_L

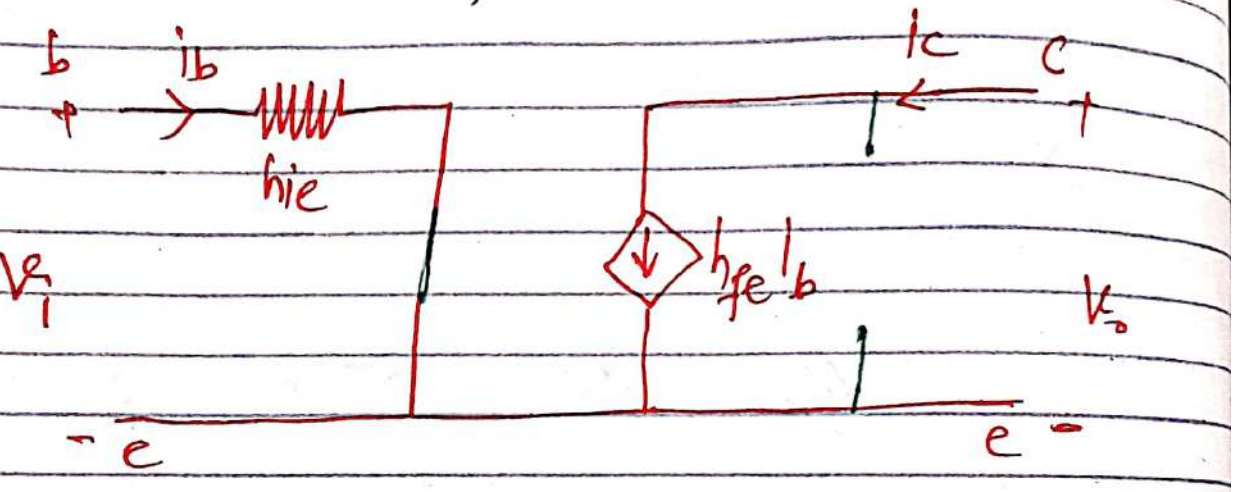
still $\frac{1}{h_o} \Rightarrow R_C \parallel R_L$

$$h_r = \frac{V_i}{V_o}$$

As $V_o \gg V_i$ $\quad h_r \approx 0$ → neglect it

$\Rightarrow h_{re} V_o \approx 0$ → short circuit

The circuit is as;



Comparing with re model.

$$h_{ie} = (\beta+1) r_e$$

and $h_{fe} = \beta$

Conversion of h Parameters

C.E conf → CB conf

? Generally provided in CE configuration

$h_{ie}, h_{re}, h_{fe}, h_{oe}$ → $h_{ib}, h_{rb}, h_{fb}, h_{ob}$

CE to CB

$$h_{ib} = \frac{h_{ie}}{1+h_{fe}} \qquad h_{rb} = \frac{h_{ie} h_{oe}}{1+h_{fe}} - h_{re}$$

$h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$ $\quad h_{ob} = \frac{h_{oe}}{1+h_{fe}}$

CE to CC

$h_{ic} = h_{ie}$ $\quad h_{rc} = 1 - h_{re}$

$h_{fc} = -(1+h_{fe})$ $\quad h_{oc} = h_{oe}$

CB to CE

$h_{ie} = \frac{h_{ib}}{1+h_{fb}}$ $\quad h_{re} = \frac{h_{ib}h_{ob}}{1+h_{fb}} - h_{rb}$

$h_{fe} = \frac{-h_{fb}}{1+h_{fb}}$ $\quad h_{oe} = \frac{h_{ob}}{1+h_{fb}}$

The r_e transistor Model

For Low frequency signal → h parameters
→ r_e model.

For high frequency signal → hybrid π model
→ y parameters.

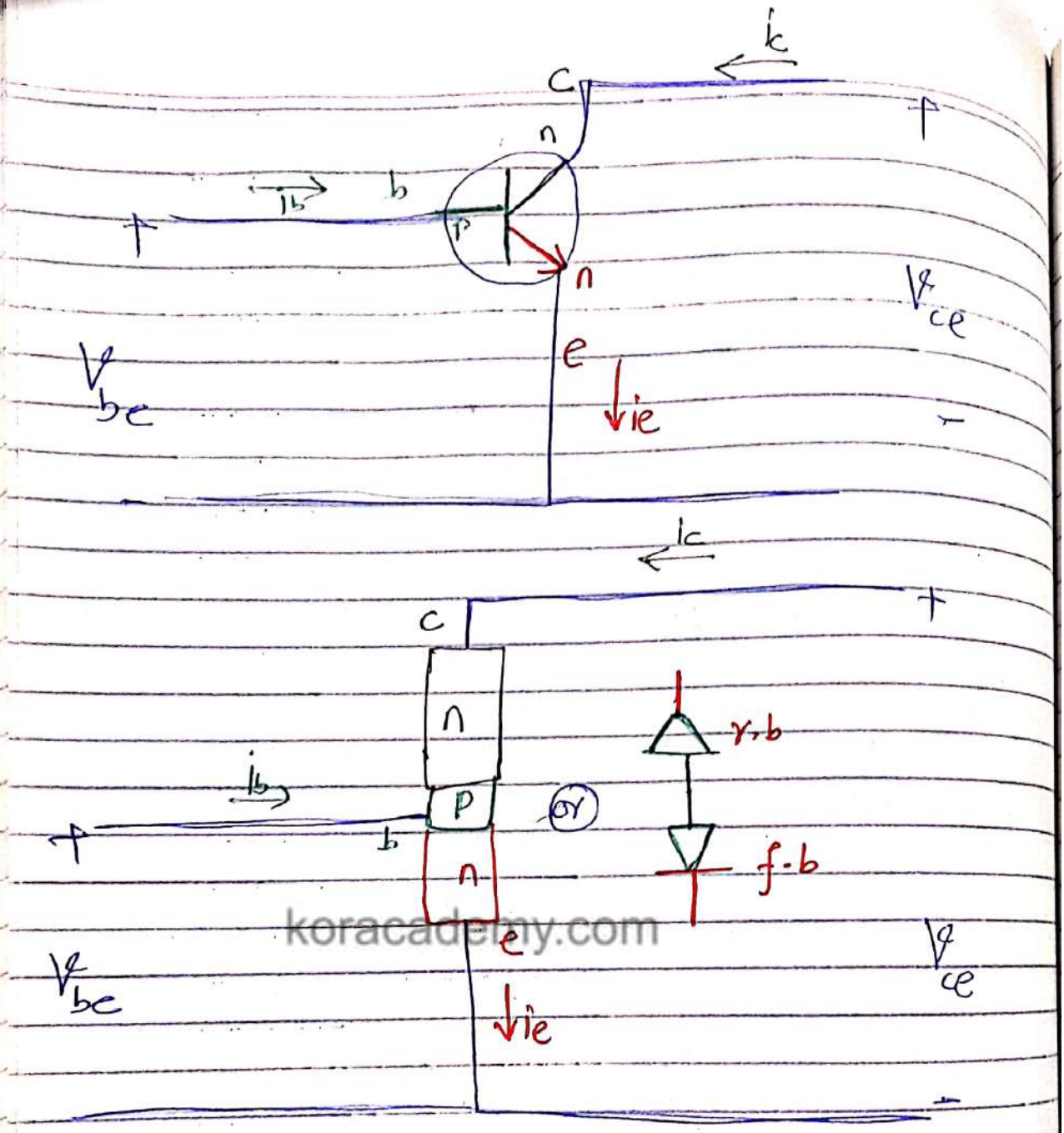
We will find out r_e model for CE transistor.

E is common to i/p and o/p side.

considering npn transistor.

i/p I = i_b $\quad$ o/p I = i_c

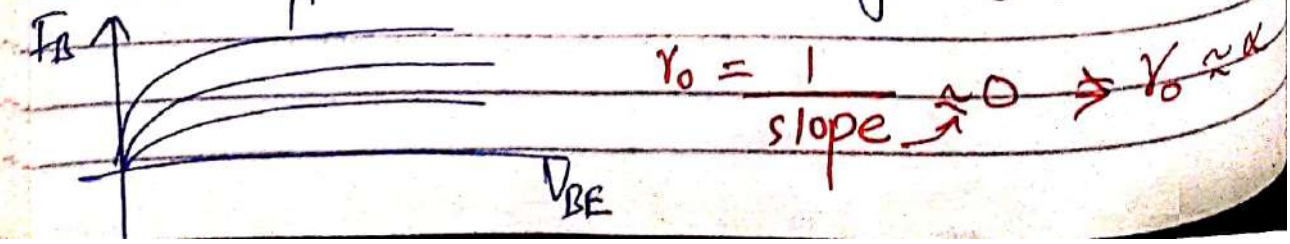
i/p V = V_{be} $\quad$ o/p V = V_{ce}



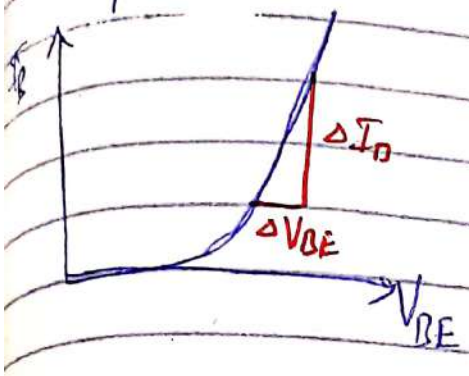
We will modify this circuit in which collector branch will have the dependent current source and the emitter branch will have the forward biased diode.

D.C.S b/c $I = i_c = \beta \cdot i_b$

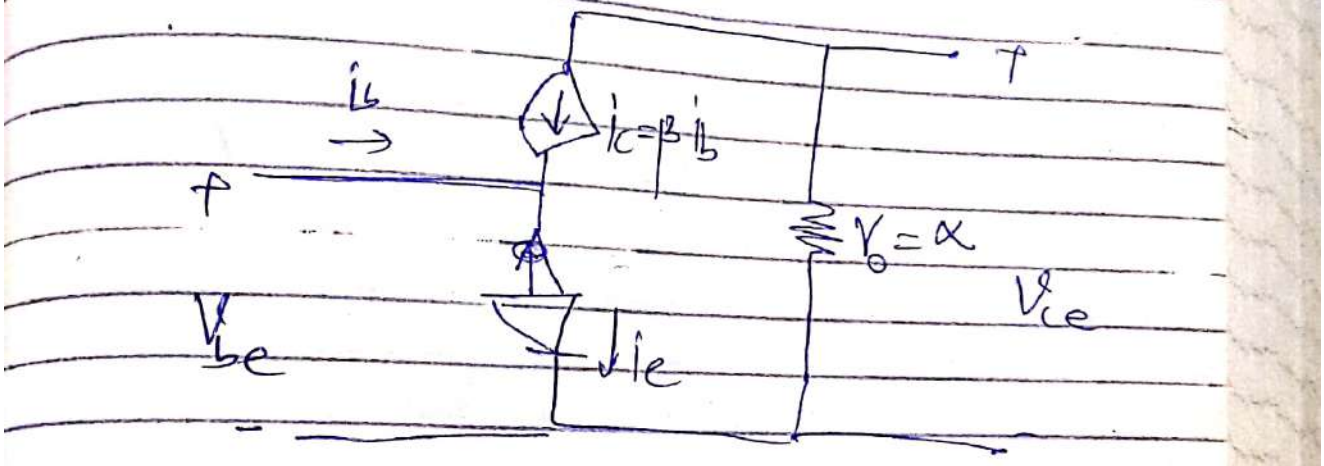
If you see the o/p characteristics of CE
⇒ o/p resistance is very large.



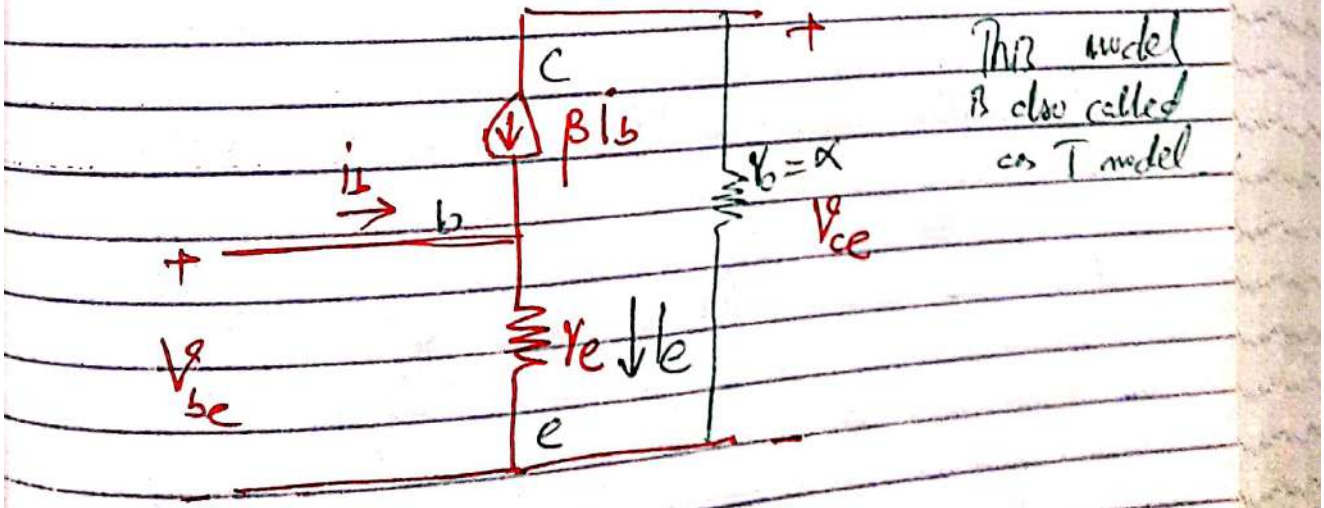
i/p chr similar to f.b diode.



$r_d = \frac{\Delta V_{BE}}{\Delta I_B}$ → i/p V
→ i/p I.



Replace the diode by dynamic resistance r_d.
(e → emitter) r_e



This model is also called as T model

Calculate of r_e?
Consider a pn junction diode with diode current = I_d and r.s.c = I_s
diode current equation $I_D = I_s\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$

$\eta = 1$ for Ge $\eta = 2$ for silicon $\Big\}$ ⇒ for low I.

$\eta = 1$ for both for high I.

$$\frac{dI_D}{dV_D} = I_S \frac{d}{dV_D}\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

$$\frac{1}{r_d} = \frac{I_S e^{V_D/V_T}}{V_T}$$

$$\frac{1}{r_d} = \frac{I_D + I_S}{V_T} \Rightarrow r_d = \frac{V_T}{I_D}$$

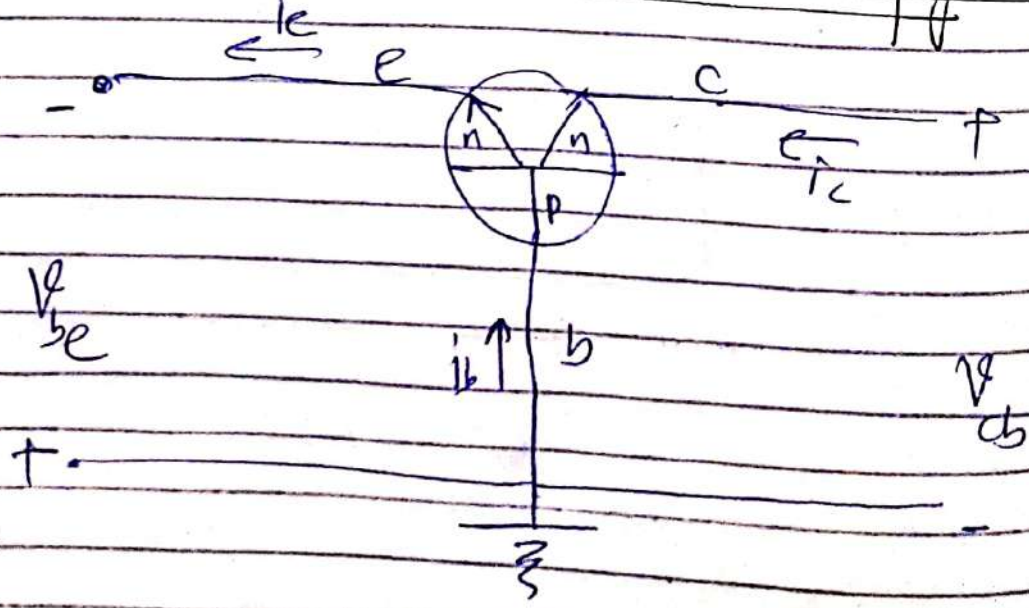
I_S = small

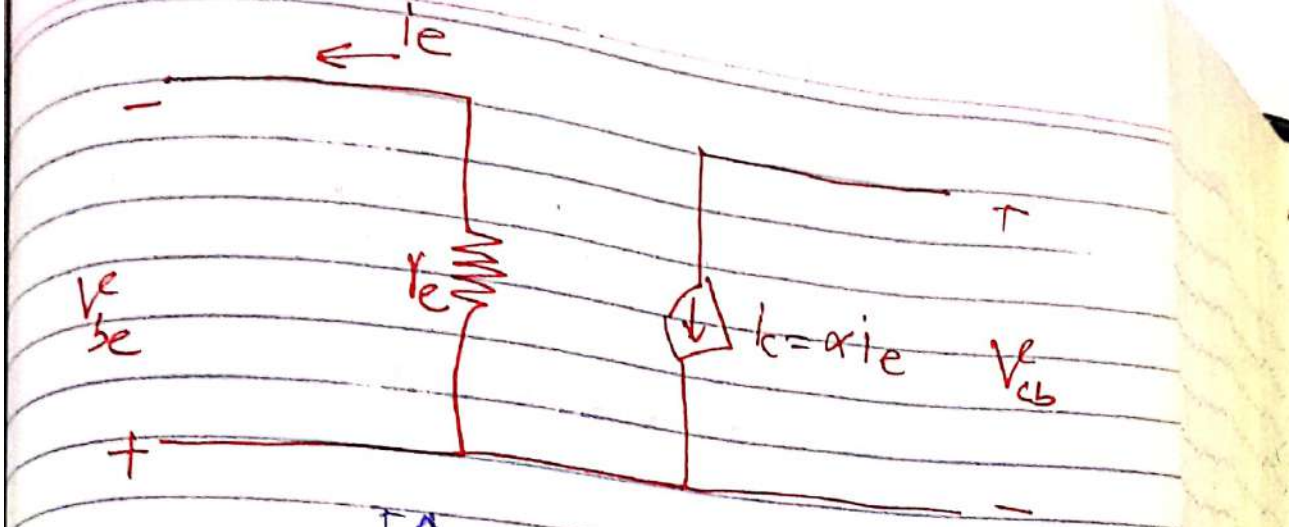
At room temperature $T = 300K \Rightarrow V_T = 26mV$

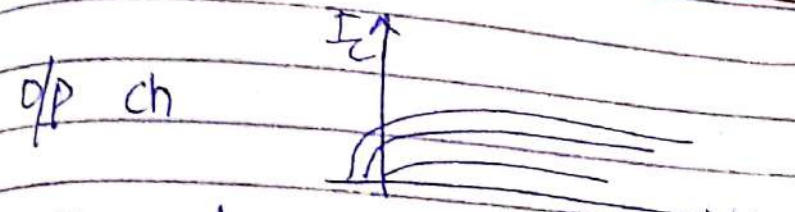
$$r_d = \frac{26mV}{I_D} \Rightarrow \boxed{r_e = \frac{26mV}{I_e}}$$

To calculate I_e, we need to draw the dc eq circuit.

Re model For Common Base Configuration







$r_o \simeq \frac{1}{\text{slope}} = \frac{1}{0} = \infty$

In C.E slope $\neq 0$

$I_B \uparrow \Rightarrow \uparrow V_{CE}$ β is large.

$r_o \neq \infty$ (but very large) (MΩ)

Modification in r_e model of CE transistor:

Try to separate i/p and o/p sides.

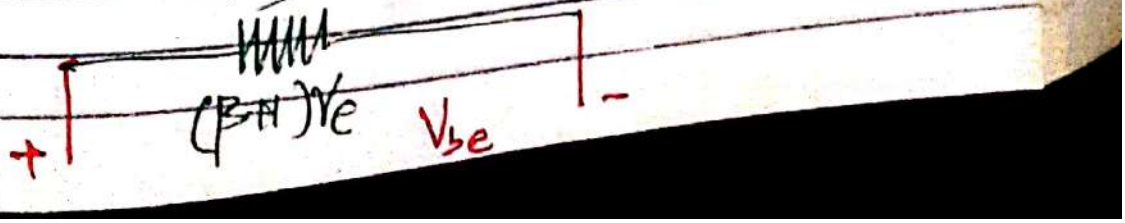
Current through $r_e = i_e$

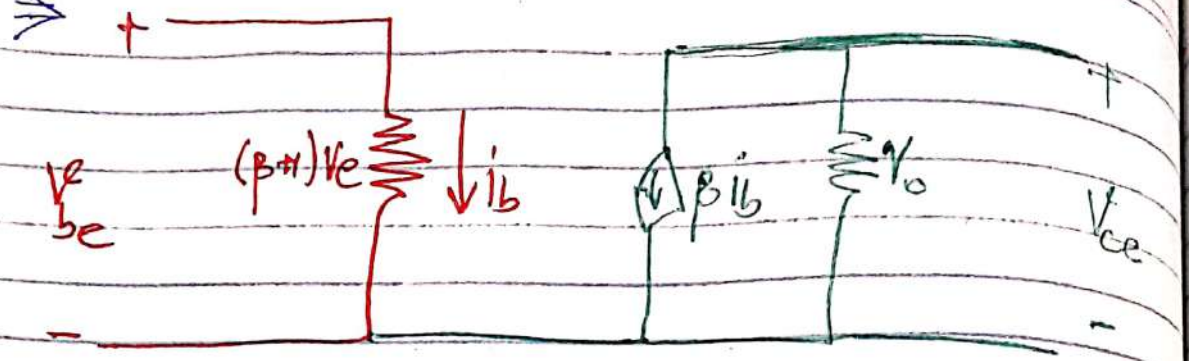
$i_e = i_c + i_b \Rightarrow \boxed{i_e = (\beta+1) i_b}$

$(i_c = \beta i_b)$

Drop across r_e? $= r_e \cdot i_e$

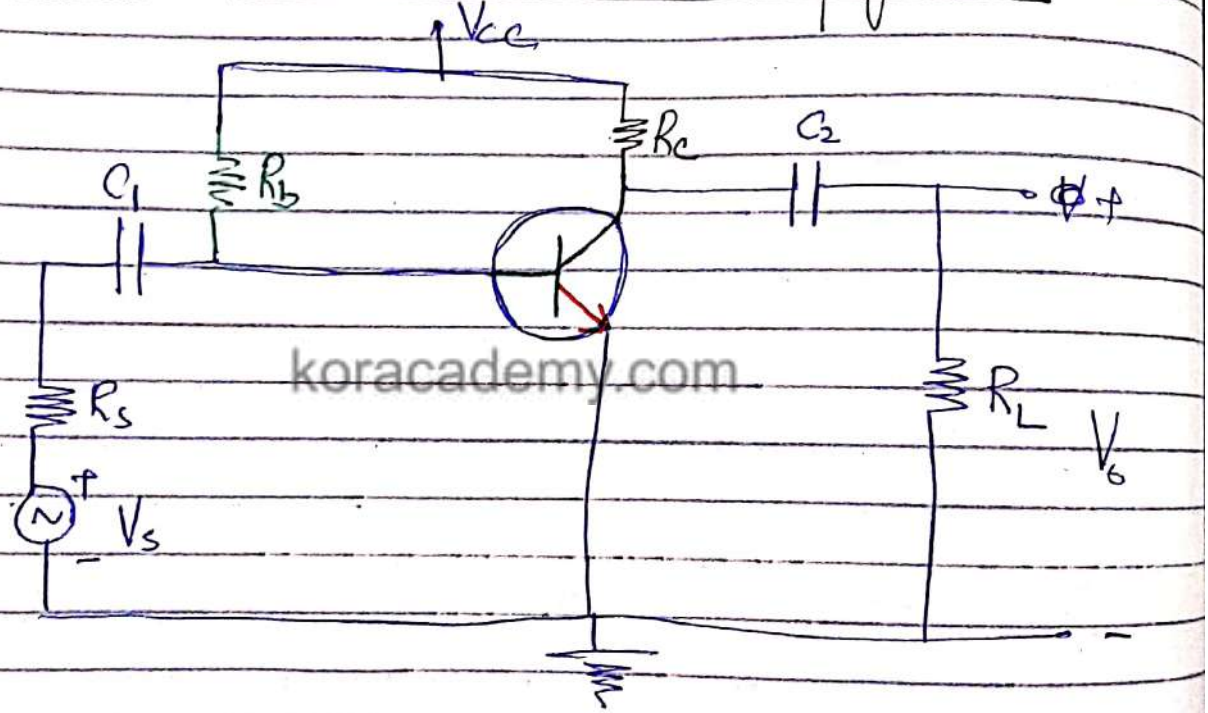
$= r_e (\beta+1)(i_b)$





$(\beta+1) \simeq \beta$

(r_e Model) CE Fixed Bias Configuration



i/p and o/p impedences?

We need to do two things.

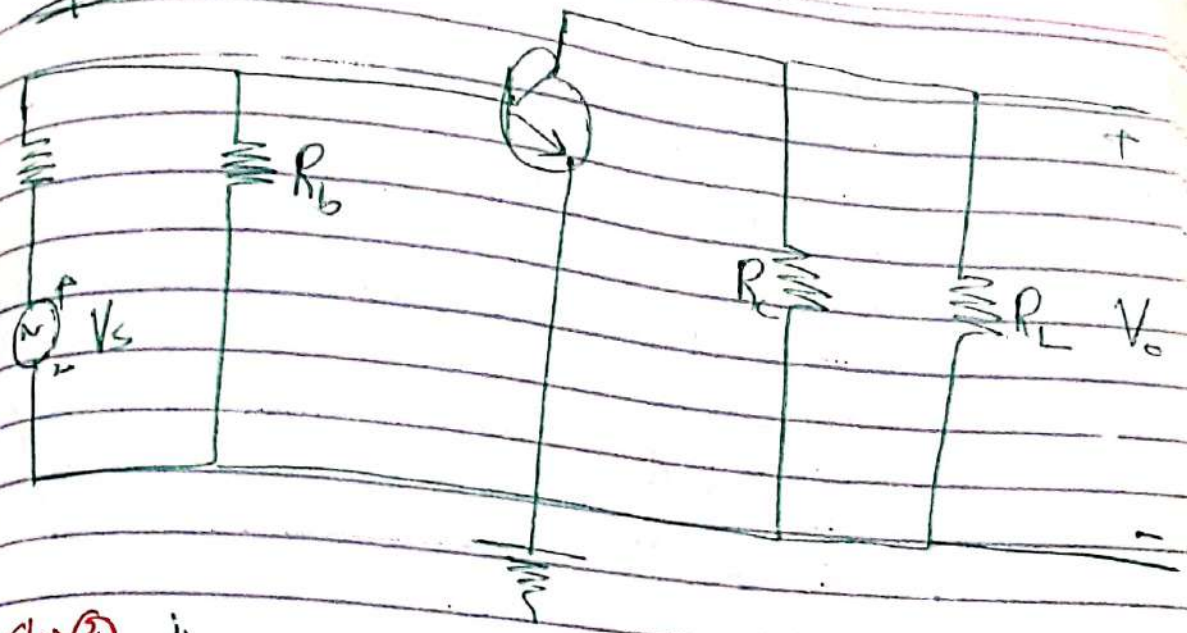
(i) Find ac equivalent circuit.

(ii) Replace the transistor with its model. (ie CE r_e model)

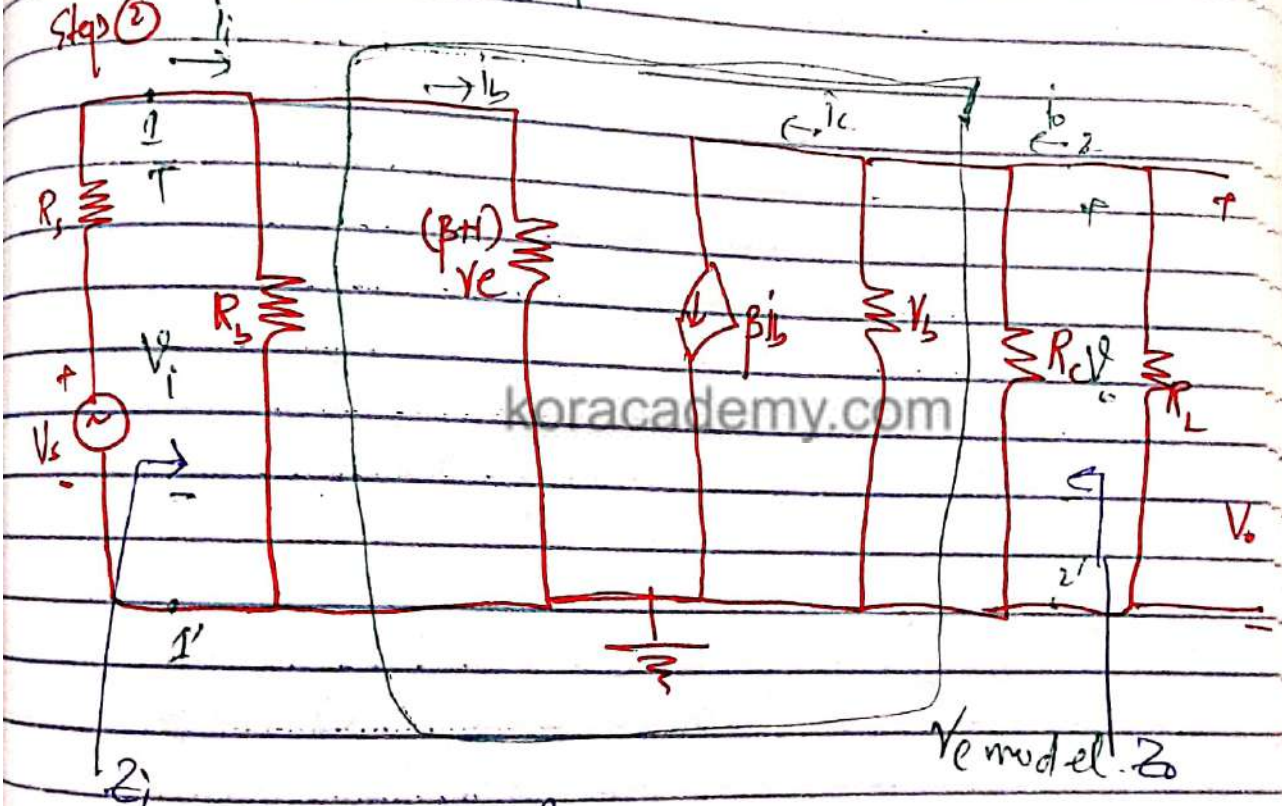
For step (i) → all the dc sources must be short circuited.

Short circuit all the capacitors

Step ①



Step ②



$$Z_i = \frac{V_i}{i_i}$$

I/p impedance is R_b in parallel with $(\beta+1) r_e$

$$Z_i = R_b \,||\, (\beta+1) r_e = \boxed{\frac{R_b (\beta+1) r_e}{R_b + (\beta+1) r_e}} \quad Z_i$$

Output impedance Z_o?

$$Z_o = \frac{V_o}{i_o}$$

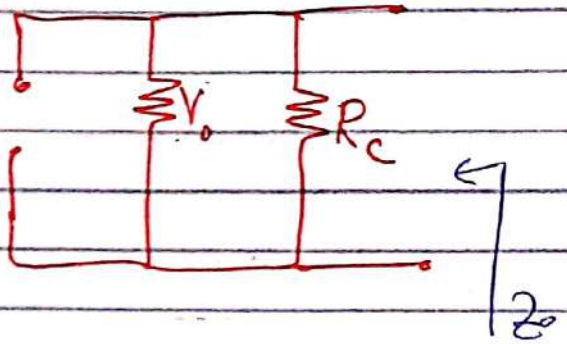
For Z_o, short circuit the source and open circuit the load.

$V_s = 0V$ $\quad R_L = \infty$

$V_i = 0V$

$i_b = 0A$

$i_c = 0A$ → current source open circuited



$$Z_o = r_o \,||\, R_c$$

$$Z_o = \frac{r_o \cdot R_c}{r_o + R_c}$$

Simplifying Z_i

$(\beta+1) \approx \beta \Rightarrow (\beta+1) r_e \approx \beta r_e$

If $R_B \geq 10(\beta+1) r_e$

↳ neglect from denominator.

$$Z_i = \frac{R_B \cdot (\beta+1) r_e}{R_B}$$

$$\boxed{Z_i = (\beta+1) r_e}$$ when $\boxed{R_B \geq 10(\beta+1) r_e}$

for Z_i

$r_o >> $ (large) $\quad r_o >> R_c$

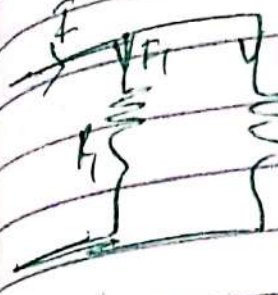
$\boxed{r_o \geq 10 R_c}$ → neglect R_c $\Rightarrow \boxed{Z_o = R_c}$

Current Gain (A_i)

$$A_i = \frac{i_o}{i_i}$$

o/p i is the current through load resistance.

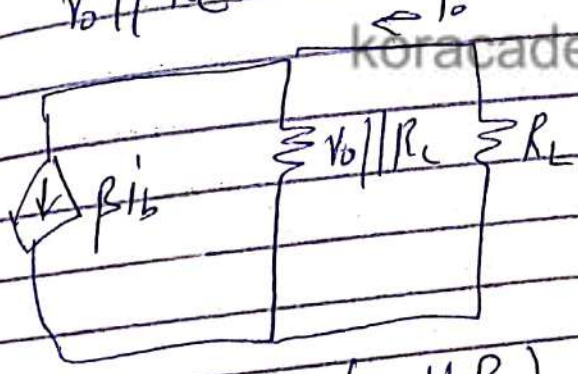
Using current divider rule;



$$I_2 = \frac{(\text{total cnt})(\text{other resnth})}{R_1 + R_2}$$

$$I_1 = \frac{I R_2}{R_1 + R_2}$$

⇒ Have a single resistance in place of $r_o \| R_C$



$$i_o = \frac{i_c (r_o \| R_C)}{(r_o \| R_C) + R_L}$$

$$A_i = \frac{\beta i_b (r_o \| R_C)}{(r_o \| R_C) + R_L} \Big/ i_i$$

C.D.R $\quad i_b = \frac{i_i R_B}{R_B + (\beta+1) r_e}$

$$A_i = \beta \left(\frac{i_i R_B}{R_B + (\beta+1) r_e} \right) \left(\frac{r_o \| R_C}{(r_o \| R_C) + R_L} \right) \Big/ i_i$$

$$A_i = \beta \left(\frac{R_B}{R_B + (\beta+1) r_e} \right) \left(\frac{r_o \| R_C}{r_o \| R_C + R_L} \right)$$

① $r_o \geq 10R_c \Rightarrow r_o \| R_c \simeq R_c$

$$A_i = \beta \left(\frac{R_B}{R_B + (\beta+1)r_e}\right)\left(\frac{R_c}{R_c + R_L}\right)$$

② R_B and $R_c \simeq \infty$ (not present)
$\Rightarrow$ no fixed bias configuration

$r_c < R_c \Rightarrow r_o \| R_c \simeq r_o$

$$A_i = \beta \left(\frac{R_B}{R_B}\right)\left(\frac{r_o}{r_o + R_L}\right)$$

$$A_i = \beta \left(\frac{r_o}{r_o + R_L}\right).$$

Overall Current Gain (A_{is})

ratio of o/p I to source I.
Similar to h parameters A_{IS}.

$$A_{IS} = \frac{i_o}{i_s} = A_i \left(\frac{R_s}{R_s + Z_i}\right)$$

Voltage Gain (A_v)

$$A_v = \frac{V_o}{V_i} = \frac{\text{o/p V}}{\text{i/p V}}$$

$V_o = ?$ $\quad V_o = -i_o R_L$

By C.D.B $\quad i_o = \dfrac{i_c (r_o \| R_c)}{r_o \| R_c + R_L}$

$i_c = \beta i_b$ $\quad V_o = -\beta i_b \left(\frac{r_o \| R_c}{r_o \| R_c + R_L} \right) R_L$

$V_i = ?$

It is the drop across R_b or $(\beta+1) r_e$

$V_i = I_b (\beta+1) r_e$

$$A_V = \frac{-\beta (r_o \| R_c \| R_L)}{(\beta+1) r_e}$$

① $\beta+1 \simeq \beta \Rightarrow A_V = \frac{-r_o \| R_c \| R_L}{r_e}$

② $r_o \geq 10 R_c \Rightarrow$ neglect r_o

$$A_V = \frac{-R_c \| R_L}{r_e}$$

③ $R_L = \infty \gg R_c$

neglect R_L

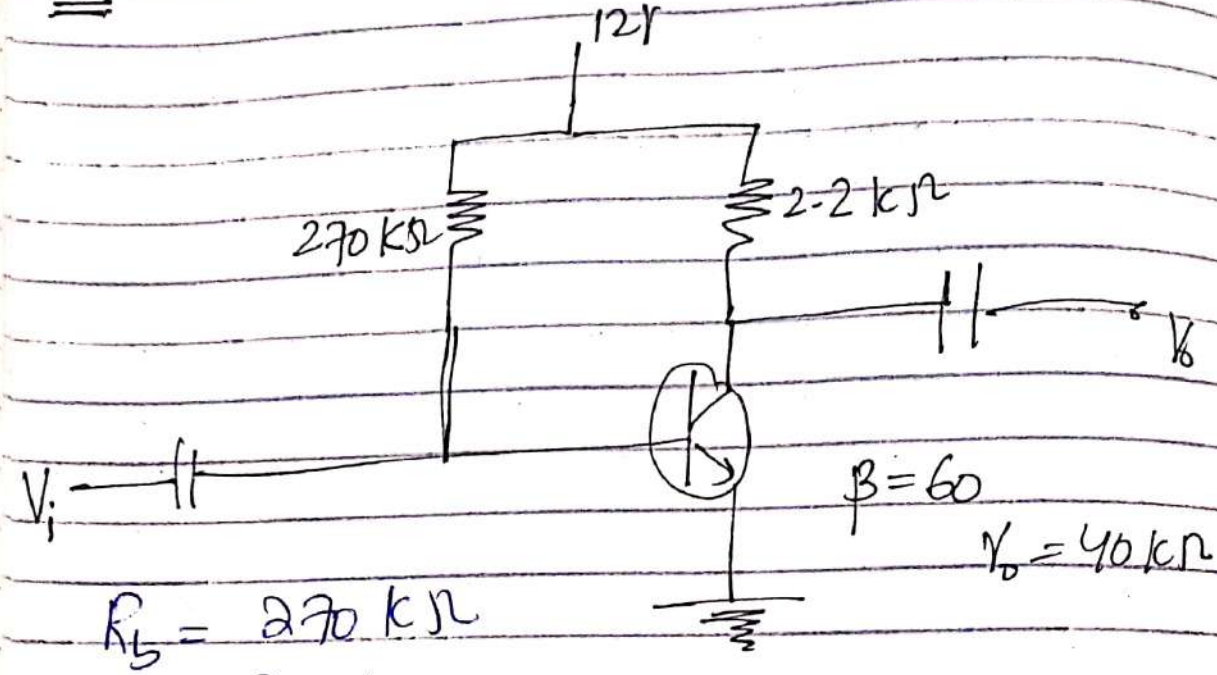
$$A_V = \frac{-R_c}{r_e}$$

The -ve sign represents 180° phase shift b/w i/p and o/p voltages.

Overall voltage gain $(A_{VS}) = \frac{V_o}{V_s}$

$$A_{VS} = A_V \left(\frac{Z_i}{Z_i + R_s} \right).$$

Q Determine Z_i and Z_o, A_v and A_i



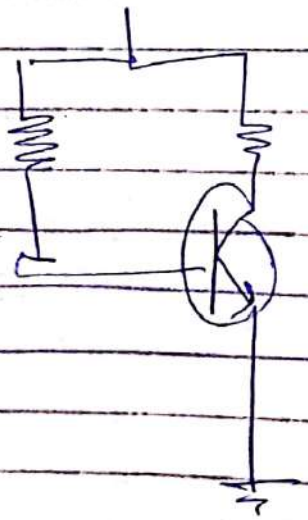
$R_B = 270\,k\Omega$

$R_C = 2.2\,k\Omega$

$r_e = ?$ $\quad r_e = \dfrac{26\,mV}{I_E}$

$I_E = ?$

dc eq circuit



$$12 - I_B R_B - V_{BE} = 0$$

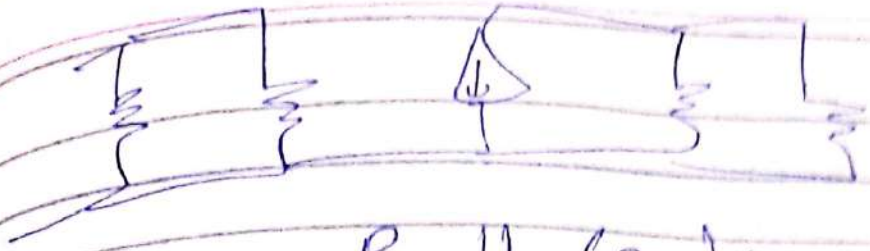
$$I_B = \frac{12 - 0.7}{220k} = 0.041\,mA = 41.8\,\mu A$$

$$I_E = (\beta + 1) I_B = (61)(41.4)$$

$$I_E = 2.55\,mA$$

$$r_e = \frac{26\,m}{2.55\,m} \Rightarrow \boxed{r_e = 10.18\,\Omega}$$

AC eq model?



$Z_i = R_B \parallel (\beta+1) r_e = \frac{R_B \cdot (\beta+1) r_e}{R_B + (\beta+1) r_e}$

$= \frac{(270k)(61)(10.18)}{270k + (61)(10.18)} \Rightarrow Z_i = 621\,\Omega$

$\approx 2\,k\Omega$

$Z_i = 0.61\,k\Omega$

$\sim 619\,k\Omega$

If $R_B \geq 10(\beta+1) r_e$

$\Rightarrow Z_i = (\beta+1) r_e$

In this case $(\beta+1) r_e = 0.62\,k\Omega$

$R_B = 270\,k\Omega$

& neglecting R_B

$\Rightarrow Z_i = 0.62 \parallel 1k\Omega \sim 621\,\Omega$

$Z_o = ?$ $\quad Z_o = r_o \parallel R_c = 2.85\,k\Omega$

$r_o \geq 10 R_c$

$Z_o = R_c = 2.2\,k\Omega$.

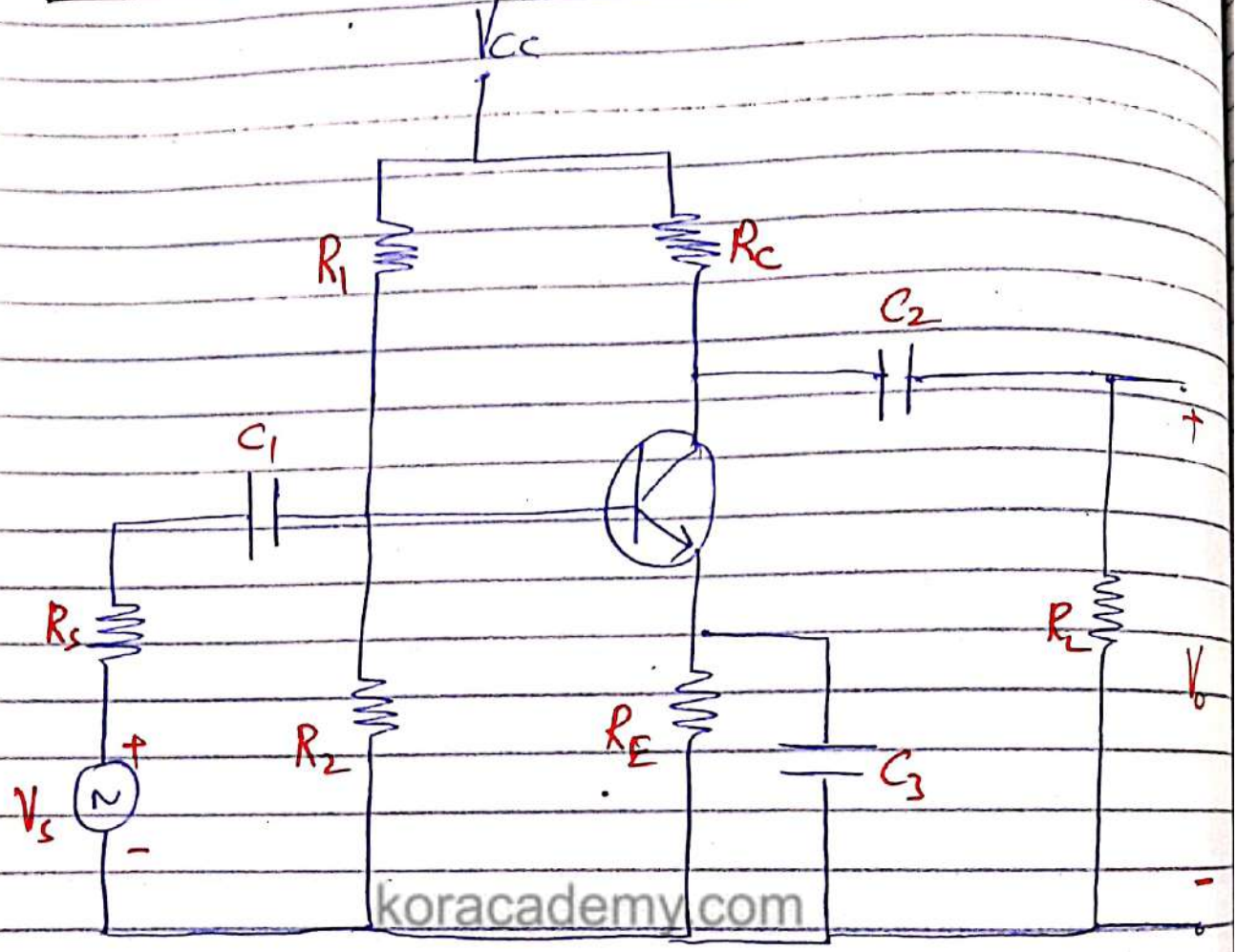
$\approx$

A_v

$A_v = \frac{-\beta i_b R_c}{i_b (\beta+1) r_e}$

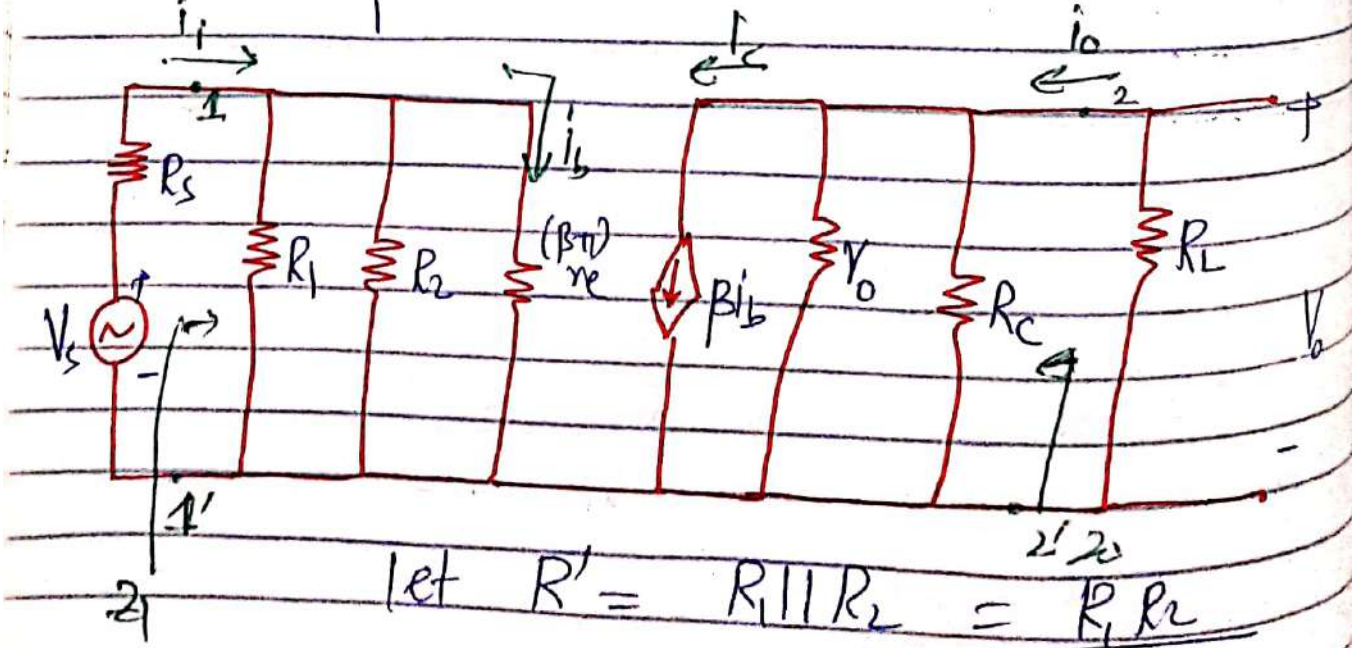
$(\beta+1) \approx \beta$ $\quad A_v = \frac{-R_c}{r_e} = -216.1$

r_e Model For Voltage Divider Bias



① AC equivalent cmit → S.C all C_s.

② r_e eq. model.



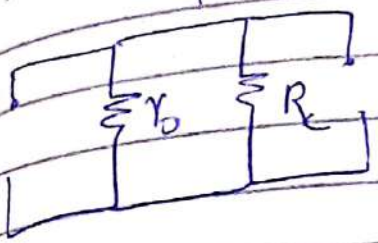
let $R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$

$Z_i = (\beta+1) r_e \| R'$

For Z_o o/c the load ie $R_L = \infty$
and S.C the source. $V_s = 0$.

$V_s = 0 \Rightarrow i_b = 0 \Rightarrow I_c = \beta i_b = 0$

So the o/p side



$$Z_o = r_o \| R_c$$

$$\Rightarrow Z_o = \frac{r_o \| R_c}{r_o + R_c}$$

If $r_o \geq 10 R_c$
r_o can be neglected.

$$\boxed{Z_o = R_c}$$

Voltage Gain

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -i_o R_L = -I_c \left(\frac{r_o \| R_c}{r_o \| R_c + R_L} \right) R_L$$

$$V_o = -\beta i_b \left(\frac{r_o \| R_c}{r_o \| R_c + R_L} \right) R_L$$

$r_o \geq 10 R_c$
Neglected r_o $\Rightarrow V_o = -\beta i_b \left(\frac{R_c}{R_c + R_L} \right) R_L$

If $R_L >> R_c$

$$V_o = -\beta i_b R_c$$

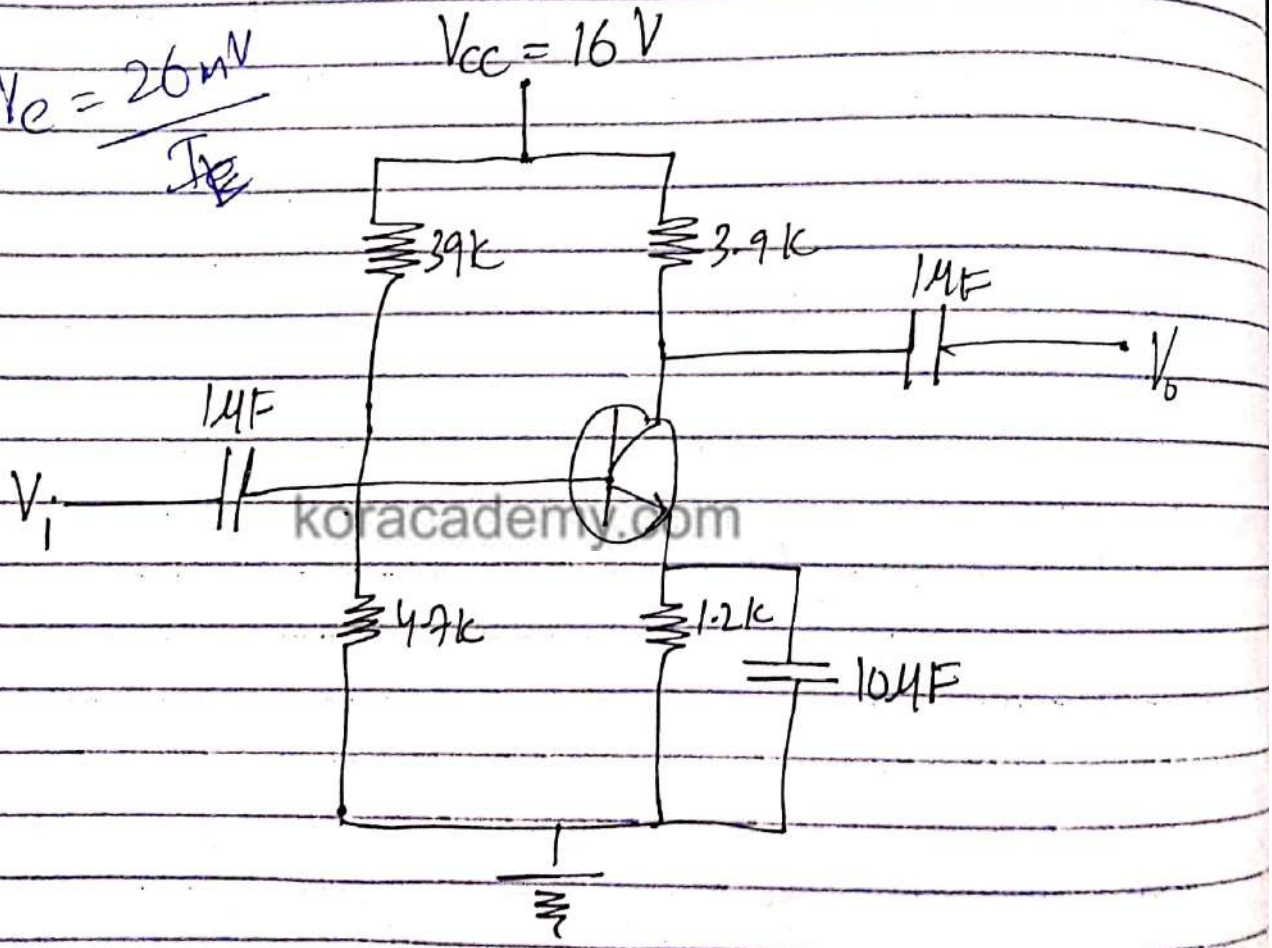
$$V_i = i_b (\beta + 1) r_e$$

$$A_V = \frac{-\beta i_b R_c}{i_b(\beta+1)r_e} \qquad A_V = \frac{-\beta R_c}{(\beta+1)r_e}$$

or $$\boxed{A_V = \frac{-R_c}{r_e}}$$

Q. Determine r_e, Z_i, Z_o, A_V, A_i.

$r_e = \frac{26mV}{I_E}$



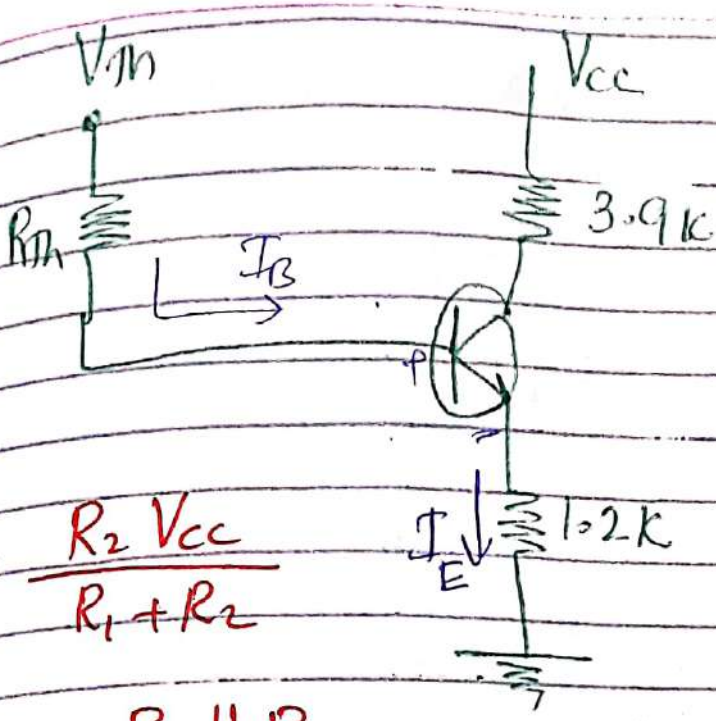
$\beta = 100$ $\quad r_o = 50\,K$ $\quad R_1 = 39k\Omega$ $\quad R_2 = 4.7k$

$R_c = 3.9k\Omega$ $\quad R_E = 1.2k\Omega$

$C_1 = 1\mu F$ $\quad C_2 = 1\mu F$ $\quad C_3 = 10\mu F$

$I_E = ?$ dc analysis. $X_c = \infty$

Thevenin eqn ckt?



$$V_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$R_{Th} = R_1 \,||\, R_2$$

$V_{Th} = 1.72\ V$ $\qquad$ $R_{Th} = 4.194\ K\Omega$

KVL to i/p loop

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E(1.2K) = 0$$

$$I_E = (\beta + 1) I_B$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1)(1.2K)} = 8.13\,\mu A$$

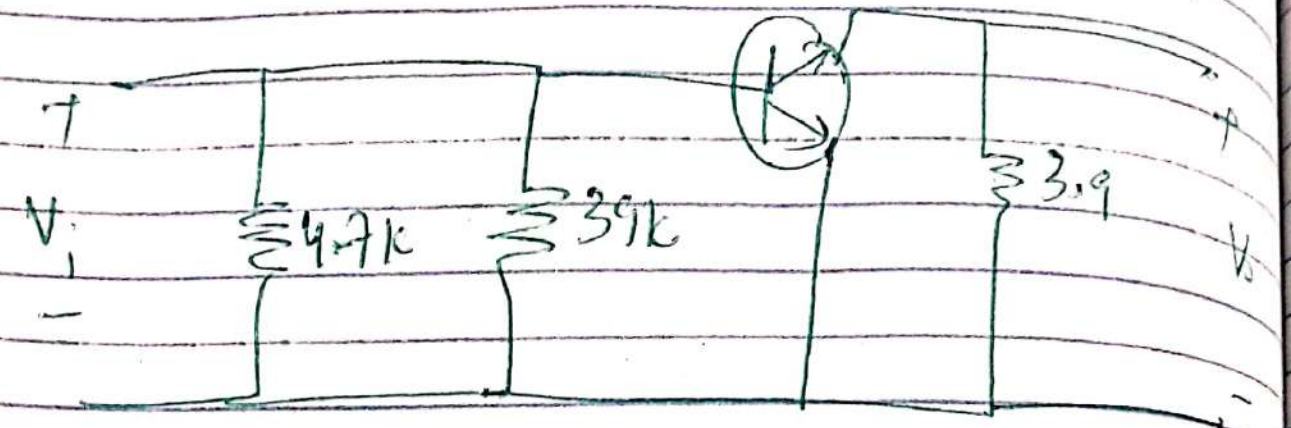
$$I_C = \beta I_B \Rightarrow I_C = 813.4\,\mu A$$

$$I_E = I_B + I_C \Rightarrow \boxed{I_E = 0.821\,mA}$$

$$r_e = \frac{26\,m}{0.821\,m} \Rightarrow \boxed{r_e = 31.6\,\Omega}$$

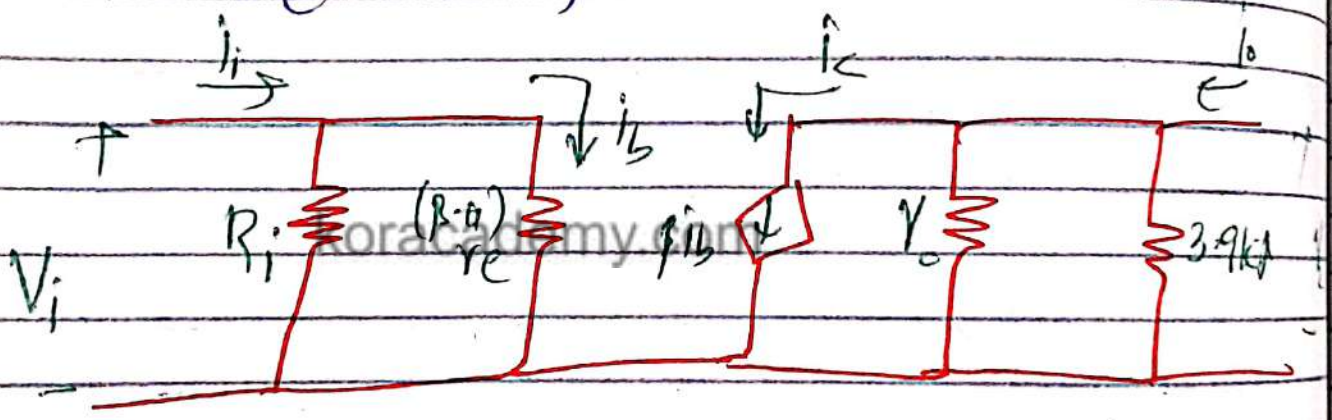
At eq. : S.C all dc sources.
S.C all capacitors $X_C = 0$

The ac equivalent circuit is as;



$R' = 4.7k \,||\, 39k = 4.19k\Omega = R_{Th}$

The r_e model;



$Z_i = R' \,||\, (\beta+1) r_e$

$(\beta+1) r_e = 3.19k\Omega$

$\Rightarrow Z_i = 1.81k\Omega$

$Z_o = r_o \,||\, 3.9k\Omega = 50 \,||\, 3.9k\Omega$

$\Rightarrow Z_o = 3.9k\Omega$

$R' \geq 10(\beta+1)r_e$ ✗

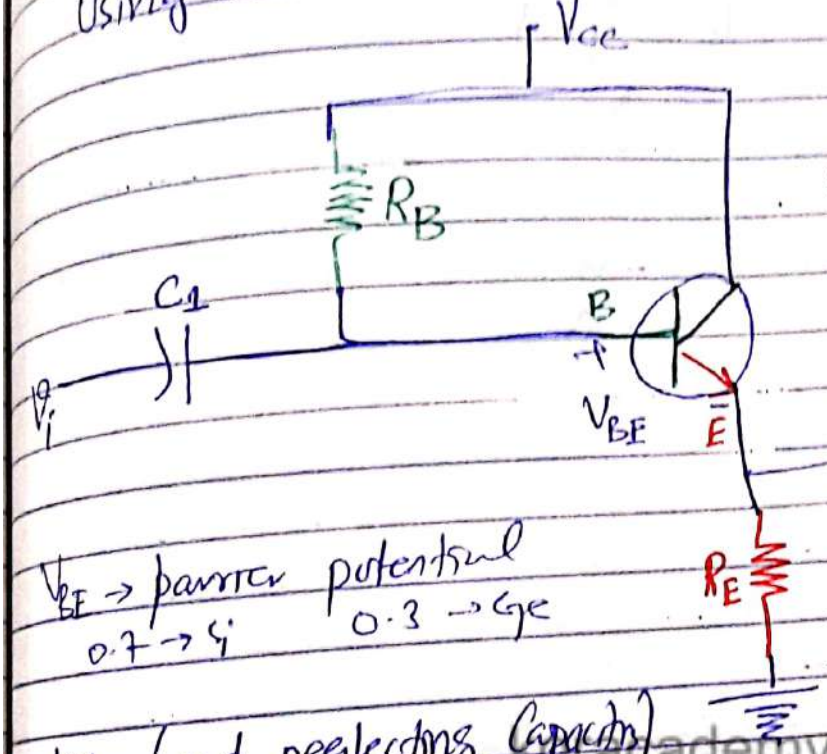
$r_o \geq 10R_C$ ✓

neglect R_o

Emitter Follower Configuration

The o/p is taken from emitter terminal instead of collector.

Using CE transistor.



V_{BE} → barrier potential
0.7 → Si
0.3 → Ge

KVL (and neglecting Capacitor)

$V_o = V_i - V_{be}$ ⓐ $V_o \simeq V_i$

Voltage Gain

$$A_V = \frac{V_o}{V_i} \simeq 1$$

Why is it called emitter follower ?

180° phase shift b/w o/p and i/p when o/p is taken from collector terminal.

When o/p is taken from emitter, it is in phase with the i/p signal. Like V_o is following V_i. They reach peak values at the same time.

AC Equivalent Ckt of E.F.C

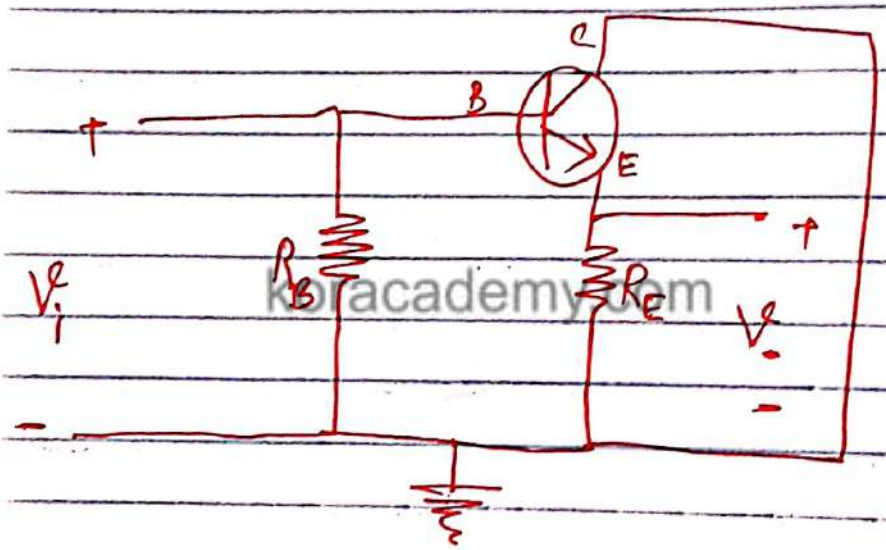
E.F.C is used for impedence matching purposes.

It provides high impedence at i/p and low impedence at o/p.

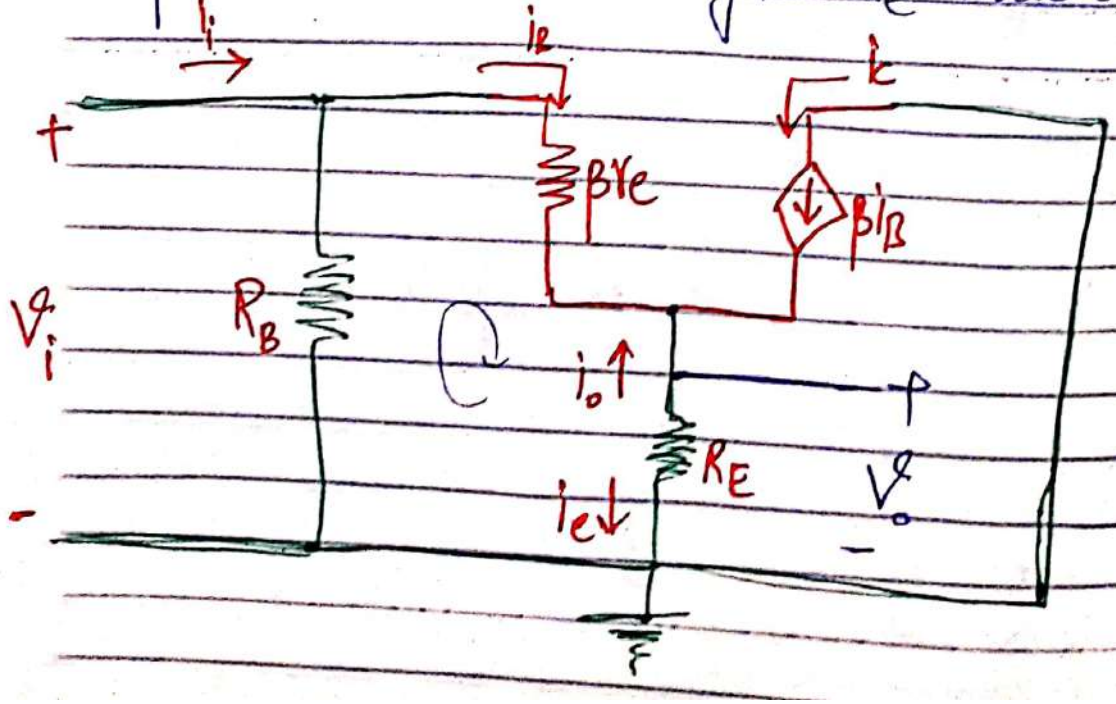
$Z_i \uparrow \quad Z_o \downarrow$ opposite to fixed bias configuration.

① Shut ckt all the dc sources. (ground is plus of the)

② Shut ckt all the capacitors.



Replace the transistor by its r_e model.



Input Impedance.

$$Z_i = R_B \parallel (\beta r_e + R_E)$$

* Current through r_e is not same as R_E

$$i_e = (\beta+1) i_b$$

drop across $R_E = i_e R_E = i_b (\beta+1) R_E$

$$Z_i = R_B \parallel (\beta r_e + (\beta+1) R_E)$$

(βr_e : i_b; $(\beta+1)R_E$: i_b)

$\beta+1 \simeq \beta$

$$Z_i = R_B \parallel (\beta r_e + \beta R_E)$$

$$Z_i = R_B \parallel \beta (r_e + R_E)$$

Generally $R_E >> r_e$ → neglect it

$$\Rightarrow Z_i = R_B \parallel \beta R_E = \frac{\beta R_E R_B}{\beta R_E + R_B}$$

Output impedance

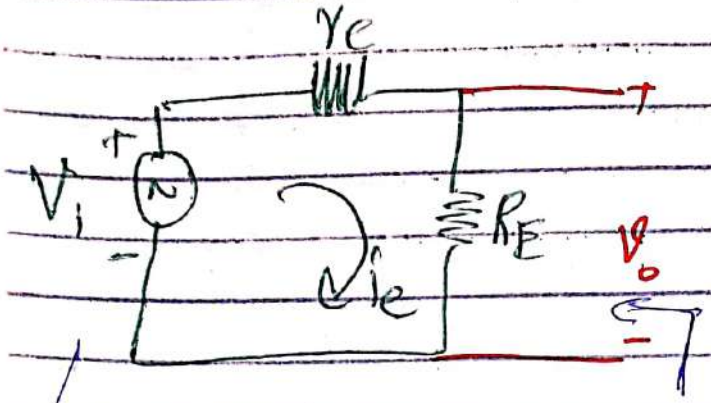
$i_e = ?$

$$i_b = \frac{V_i}{\beta r_e + \beta R_E}$$

$$i_e = (\beta+1) i_b$$

$$i_e = \frac{(\beta+1) V_i}{\beta r_e + \beta R_E} \qquad \beta+1 \simeq \beta$$

$$I_e = \frac{V_i}{r_e + R_E}$$



For Z_o $V_i = 0V$ short cct.

$$Z_o = r_e \| R_E$$

$$Z_o = \frac{r_e R_E}{r_e + R_E}$$

Generally

$R_E >> r_e$ ↳ neglecting from denomi.

$$Z_o = \frac{r_e R_E}{R_E}$$

$$Z_o = r_e$$

Voltage Gain (A_v).

$$A_v = \frac{V_o}{V_i}$$

$$V_o = I_e R_E = \left(\frac{V_i}{r_e + R_E}\right)$$

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{r_e + R_E}$$

$R_E >> r_e$ neglect from denom.

$A_v \simeq 1$.